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UTILITY PATENT APPLICATION TRANSMITTAL		Attorney Docket No. 98-1068.02	Total Pages
(Only for new non-provisional applications under 37 CFR 1.53(b))		First Named Inventor or Application Identifier D. Mark Durcan et al.	
		Express Mail Label No.	EL003000628US

APPLICATION ELEMENTS See MPEP chapter 600 concerning utility patent application contents.		ADDRESS TO: Assistant Commissioner for Patents Box Patent Application Washington, DC 20231	
1. <input checked="" type="checkbox"/> Fee Transmittal Form (Submit an original, and a duplicate for fee processing)	6. <input type="checkbox"/> Microfiche Computer Program (Appendix)		
2. <input checked="" type="checkbox"/> Specification Total Pages <u>45</u> (preferred arrangement set forth below) -Descriptive -Cross References to Related Application -Statement Regarding Fed sponsored R & D -Reference to Microfiche Appendix -Background of the Invention -Brief Summary of the Invention -Brief Description of the Drawings (if filed) -Detailed Description -Claim(s) -Abstract of the Disclosure	7. Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary) a. <input type="checkbox"/> Computer Readable Copy b. <input type="checkbox"/> Paper Copy (identical to computer copy) c. <input type="checkbox"/> Statement verifying identity of above copies		
3. <input checked="" type="checkbox"/> Drawing(s) (35 USC 113) Total Sheets <u>159</u> Total Pages <u>53</u>	ACCOMPANYING APPLICATION PARTS		
4. Oath or Declaration a. <input type="checkbox"/> Newly executed (original or copy) b. <input checked="" type="checkbox"/> Copy from a prior application (37CFR 1.63(d)) (for continuation/divisional with Box 17 completed) [Note Box 5 below] i. <input checked="" type="checkbox"/> DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).	8. <input type="checkbox"/> Assignment Papers (cover sheet & document(s))	9. <input checked="" type="checkbox"/> 37 CFR 3.73(b) Statement <input checked="" type="checkbox"/> Power of Attorney (where there is an assignee)	
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	14. <input type="checkbox"/> Small Entity <input type="checkbox"/> Statement filed in prior application Statement(s) Status still proper and desired	15. <input type="checkbox"/> Certified Copy of Priority Document(s) (if foreign priority is claimed)	
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NAME	Charles Brantley Micron Technology, Inc.		
ADDRESS	8000 S. Federal Way Mail Stop 525		
CITY	Boise	STATE	Idaho
COUNTRY	USA	TELEPHONE	(208) 368-4557
		Fax	(208) 368-5606

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FEE TRANSMITTAL		Complete if Known	
		Application Number	
		Filing Date	August 31, 2000
		First Named Inventor	D. Mark Durcan et al.
		Group Art Unit	
		Examiner Name	
TOTAL AMOUNT OF PAYMENT	(\$) 690	Attorney Docket Number	98-1068.02

METHOD OF PAYMENT (check one)		FEE CALCULATION (continued)																																																																																																																																																																															
<p>1. <input checked="" type="checkbox"/> The Commissioner is hereby authorized to charge indicated fees and credit any over payments to.</p> <p>Deposit Account Number 13-3092, Order No. 98-1068.02</p> <p>Deposit</p> <p>Account Name Micron Technology, Inc.</p> <p><input checked="" type="checkbox"/> Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17 <input type="checkbox"/> Charge the Issue Fee Set in 37 CFR 1.18 at the Mailing of the Notice of Allowance, 37 CFR 1.31(b)</p> <p>2. <input type="checkbox"/> Payment Enclosed: <input type="checkbox"/> Check <input type="checkbox"/> Money Order <input type="checkbox"/> Other</p>		<p>3. ADDITIONAL FEES</p> <table border="1"><thead><tr><th>Large Fee Code</th><th>Entity Fee (\$)</th><th>Small Fee Code</th><th>Entity Fee (\$)</th><th>Fee Description</th><th>Fee Paid</th></tr></thead><tbody><tr><td>105</td><td>130</td><td>205</td><td>65</td><td>Surcharge - late filing fee or oath</td><td></td></tr><tr><td>127</td><td>50</td><td>227</td><td>25</td><td>Surcharge - late provisional filing or cover sheet.</td><td></td></tr><tr><td>139</td><td>130</td><td>139</td><td>130</td><td>Non-English specification</td><td></td></tr><tr><td>147</td><td>2,520</td><td>147</td><td>2,520</td><td>For filing a request for reexamination</td><td></td></tr><tr><td>112</td><td>920*</td><td>112</td><td>920*</td><td>Requesting publication of SIR prior to Examiner action</td><td></td></tr><tr><td>113</td><td>1,840*</td><td>113</td><td>1,840*</td><td>Requesting publication of SIR after Examiner action</td><td></td></tr><tr><td>115</td><td>110</td><td>215</td><td>55</td><td>Extension for response within first month</td><td></td></tr><tr><td>116</td><td>400</td><td>216</td><td>200</td><td>Extension for response within second month</td><td></td></tr><tr><td>117</td><td>950</td><td>217</td><td>475</td><td>Extension for response within third month</td><td></td></tr><tr><td>118</td><td>1,570</td><td>218</td><td>755</td><td>Extension for response within fourth month</td><td></td></tr><tr><td>119</td><td>310</td><td>219</td><td>155</td><td>Notice of Appeal</td><td></td></tr><tr><td>120</td><td>310</td><td>220</td><td>155</td><td>Filing a brief in support of an appeal</td><td></td></tr><tr><td>121</td><td>270</td><td>221</td><td>135</td><td>Request for oral hearing</td><td></td></tr><tr><td>138</td><td>1,510</td><td>138</td><td>1,510</td><td>Petition to institute a public use proceeding</td><td></td></tr><tr><td>140</td><td>110</td><td>240</td><td>55</td><td>Petition to revive unavoidably abandoned application</td><td></td></tr><tr><td>141</td><td>1,320</td><td>241</td><td>660</td><td>Petition to revive unintentionally abandoned application</td><td></td></tr><tr><td>142</td><td>1,320</td><td>242</td><td>660</td><td>Utility issue fee (or reissue)</td><td></td></tr><tr><td>143</td><td>450</td><td>243</td><td>225</td><td>Design issue fee</td><td></td></tr><tr><td>144</td><td>670</td><td>244</td><td>335</td><td>Plant issue fee</td><td></td></tr><tr><td>122</td><td>130</td><td>122</td><td>130</td><td>Petitions to the Commissioner</td><td></td></tr><tr><td>123</td><td>50</td><td>123</td><td>50</td><td>Petitions related to provisional applications</td><td></td></tr><tr><td>126</td><td>240</td><td>126</td><td>240</td><td>Submission of Information Disclosure Stmt</td><td></td></tr><tr><td>581</td><td>40</td><td>581</td><td>40</td><td>Recording each patent assignment per property (times number of properties)</td><td>0</td></tr><tr><td>146</td><td>790</td><td>246</td><td>395</td><td>Filing a submission after final rejection (37 CFR 1.129(a))</td><td></td></tr><tr><td>149</td><td>790</td><td>249</td><td>395</td><td>For each additional invention to be examined (37 CFR 1.129(b))</td><td></td></tr><tr><td colspan="4">Other fee (specify) _____</td><td></td><td></td></tr><tr><td colspan="4">Other fee (specify) _____</td><td></td><td></td></tr><tr><td colspan="4">SUBTOTAL (3)</td><td></td><td>(\$) 0</td></tr></tbody></table>		Large Fee Code	Entity Fee (\$)	Small Fee Code	Entity Fee (\$)	Fee Description	Fee Paid	105	130	205	65	Surcharge - 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SUBMITTED BY		Complete (if applicable)	
Typed or Printed Name	Charles Brantley	Reg. Number	38,086
Signature	Charles Brantley	Date	8/30/00
		Deposit Acct User ID	13-3092, ORDER NO. 98-1068 02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: D. Mark Durcan, et al.

Serial No.:

Filed: August 31, 2000

For: CONTAINER CAPACITOR STRUCTURE AND
METHOD OF FORMATION THEREOF

§
§ Group Art Unit:
§
§ Examiner:
§
§ Atty. Docket: 98-1068.02
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PRELIMINARY AMENDMENT

Assistant Commissioner for Patents

Washington, D.C. 20231

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Signature

After awarding the above-captioned application the benefit of the priority date of its parent -
- application #09/389,866, filed September 2, 1999 -- please amend the current application as
follows.

IN THE SPECIFICATION:

Immediately after the title, please add the following: --

Related Application

This application is a divisional of pending U.S. application Ser. No. 09/389,866, filed Sept.
2, 1999. --

IN THE CLAIMS:

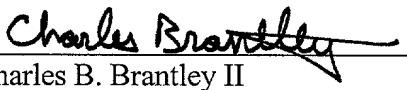
Please cancel claims 1-28 and 30-66 without prejudice.

REMARKS

Claim 29 is the only claim pending as of this Preliminary Amendment. In a restriction requirement issued as part of the Office Action of May 18, 2000 during prosecution of the parent application, the Examiner identified this claim as a "Group II" claim "drawn to a method of making a container capacitor, classified in class 438, subclass 387." Applicants have deleted an inventor accordingly. If there are any matters which may be resolved or clarified through a telephone interview, the Examiner is requested to contact Applicants' undersigned attorney at the number indicated.

Respectfully submitted,

Date: 8/31/00


Charles B. Brantley II
Reg. No. 38,086
Micron Technology, Inc.
8000 S. Federal Way
Boise, ID 83716-9632
(208) 368-4557
ATTORNEY FOR APPLICANTS

DOCKET NO.: 98-1068

APPLICATION FOR LETTERS PATENT

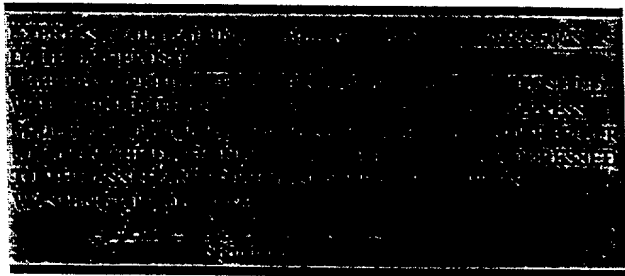
FOR

CONTAINER CAPACITOR STRUCTURE
AND METHOD OF FORMATION THEREOF

INVENTORS:

D. Mark Durcan
Trung T. Doan
Roger R. Lee
Fernando González
Er-Xuan Ping

Charles Brantley, Reg. No. 38,086
Micron Technology, Inc.
8000 S. Federal Way
Boise, ID 83716-9632
(208) 368-4557



CONTAINER CAPACITOR STRUCTURE
AND METHOD OF FORMATION THEREOF

ABSTRACT OF THE DISCLOSURE

5

Disclosed is a container capacitor structure and method of constructing it. An etch mask and etch are used to expose portions of an exterior surface of electrode ("bottom electrodes") of the container capacitor structure. The etch provides a recess between proximal pairs of container capacitor structures, which recess is available for forming additional capacitance. Accordingly, a capacitor dielectric and a top electrode are formed on and adjacent to, respectively, both an interior surface and portions of the exterior surface of the first electrode. Advantageously, surface area common to both the first electrode and second electrodes is increased over using only the interior surface, which provides additional capacitance without a decrease in spacing for clearing portions of the capacitor dielectric and the second electrode away from a contact hole location. Furthermore, such clearing of the capacitor dielectric and the second electrode portions may be done at an upper location of a substrate assembly in contrast to clearing at a bottom location of a contact via.

CONTAINER CAPACITOR STRUCTURE AND METHOD OF FORMATION THEREOF

5 FIELD OF THE INVENTION

The present invention relates generally to capacitor structures, and more particularly to capacitor container structures for dense memory arrays.

BACKGROUND OF THE INVENTION

10 Advances in miniaturization of integrated circuits have led to smaller areas available for devices such as transistors and capacitors. For example, in semiconductor manufacture of a memory array for a dynamic random access memory (DRAM), each memory cell comprises a capacitor and a transistor. In a conventional DRAM, pairs of memory cells are located within regions ("memory cell areas") defined by intersecting
15 row lines ("word lines") and column lines ("bit lines" or "digit lines"). Accordingly, to increase memory cell density of the memory array, row lines and column lines are positioned with minimal spacing ("pitch"). Using minimal pitch in turn constrains memory cell area.

In conflict with reducing memory cell area is maintaining a sufficient amount of
20 memory cell charge storage capacitance. Each DRAM memory comprises a capacitor for storing charge. A capacitor is two conductors separated by a dielectric, and its capacitance, C, is mathematically determinable as:

$$C=(\epsilon_r\epsilon_0 A)/d,$$

where ϵ_0 is a physical constant; dielectric constant, ϵ_r , is a material dependant property;

distance, d , is distance between conductors; and area, A , is common surface area of the two conductors.

Thus, to increase capacitance, C , by increasing area, A , the DRAM industry has shifted from planar capacitor structures (e.g., "parallel plate capacitors") to vertical capacitor structures (e.g., "container capacitors"). As suggested by its name, one version of a "container capacitor" may be envisioned as including cup-shape electrodes, one stacked within the other, separated by a dielectric layer or layers. Accordingly, a container capacitor structure provides more common surface area, A , within a memory cell area than its planar counterpart, and thus, container capacitors do not have to occupy as much memory cell area as their planar counterparts in order to provide an equivalent capacitance.

To increase a container capacitor's capacitance, others have suggested etching to expose exterior surface 9 of capacitor bottom electrode 20 all around each in-process container capacitor 8A, as illustratively shown in the top plan view of FIG. 1 and in the cross-sectional view of FIG. 2. This is in contrast to the conventional approach of only using interior surface 2, as illustratively shown in the cross-sectional view of FIG. 3.

With respect to FIG. 2, capacitor dielectric layer 23A and capacitor top electrode layer 24A are deposited on interior surface 2 and exterior surface 9 of capacitor bottom electrode 20. With respect to FIG. 3, capacitor dielectric layer 23B and capacitor top electrode layer 24B are deposited on interior surface 2 of capacitor bottom electrode 20. Accordingly, surface area, A , of container capacitor 8A of substrate assembly 10A will be greater than that of container capacitor 8B of substrate assembly 10B. By substrate assembly as used herein, it is meant a substrate having one or more layers formed thereon

or therein. Moreover, in the current application, the term “substrate” or “semiconductor substrate” will be understood to mean any construction comprising semiconductor material, including but not limited to bulk semiconductive materials such as a semiconductor wafer (either alone or in assemblies comprising other materials thereon),
5 and semiconductive material layers (either alone or in assemblies comprising other materials). Further, the term “substrate” also refers to any supporting structure including, but not limited to, the semiconductive substrates described above.

Container capacitor 8A poses problems for high-density memory array architectures. By high-density memory array architecture, it is meant a memory array
10 with a bit line-to-bit line pitch equal to or less than 0.5 microns. Combined thickness of capacitor dielectric layer 23A and top capacitor electrode layer 24A is approximately 50 nm to 150 nm, and space 7 between capacitor bottom electrodes 20 exterior surface 9 and the contact site 5, indicated by dashed-lines, is approximately 200 nm or less. The contact site 5 designates a contact's current or eventual location. Forming capacitor dielectric
15 layer 23A and top capacitor electrode layer 24A all around exterior surface 9 of capacitor bottom electrodes 20 encroaches upon nearby contact sites 5. While not wishing to be bound by theory, it is believed that this causes an increase in shorts between container capacitor 8A and contacts. This shorting may be due to diffusion and/or stress migration of material from capacitor top electrode layer 24A to one or more contacts. Moreover,
20 such shorting may be due to residue left from a contact etch, as is explained below with respect to substrate assembly 10A.

With respect to substrate assembly 10A of FIG. 2, dielectric layer 60A is deposited on capacitor top electrode layer 24A, and then etch mask 61 is deposited and patterned for

etching a contact via at the contact site 5. However, to provide the contact via, a portion of capacitor top electrode layer 24A and a portion of dielectric layer 23A at the bottom of the contact via must be cleared. Clearing materials at the bottom of a contact via is more problematic than clearing them at the top where they are more accessible. For example, a photo processes may not be tolerant enough to clear material from the bottom of the via given the via's diameter and depth.

In substrate assembly 10B of FIG. 3, dielectric layer 60B is deposited before deposition of capacitor top electrode layer 24B and dielectric layer 23B. Accordingly, those portions of capacitor top electrode layer 24B and dielectric layer 23B to be cleared for forming a contact via at the contact site 5 are more accessible than their counterparts in substrate assembly 10A.

Thus, there is a need in the art of container capacitors to provide a structure and process therefor which increases capacitance with less likelihood of the above-mentioned problems of shorts. Such structures and processes should also be more able to accommodate process limitations such as photo tolerance.

SUMMARY OF THE INVENTION

Accordingly, the embodiments of the present invention provide capacitor structures and methods for forming them. One exemplary apparatus embodiment includes a cup-shaped bottom electrode defining an interior surface and an exterior surface. A capacitor dielectric is disposed on the interior surface and on portions of the exterior surface. A top electrode is also disposed on the interior surface and on portions of the exterior surface. An insulating layer contacts other portions of the bottom electrode's

exterior surface. The top electrode is not deposited between a contact and surrounding bottom electrodes due to the presence of the insulating layer.

Other exemplary apparatus embodiment concern a memory array and, more particularly, a high-density memory array structure. In one exemplary embodiment of this type, a portion of a memory array comprises a contact surrounded by a plurality of container capacitors. Each capacitor has a cup-shaped bottom electrode, a dielectric, and a top electrode. Further, each contact is separated from each bottom electrode by a buffer material such as an insulating layer. Recesses between adjacent bottom electrodes are formed in the insulating layer, and a capacitor dielectric layer and top electrode layer are deposited in those recesses.

Other exemplary embodiments include methods for forming at least one capacitor. One such exemplary embodiment includes providing a plurality of cup-shaped bottom electrodes. A recess or trench between adjacent bottom electrodes is formed, thereby exposing a portion of the adjacent bottom electrodes' exterior surfaces. A capacitor dielectric is deposited at the interior of the cup-shaped bottom electrode as well as the interior of the recess. A top electrode is then deposited in the interior of the cup-shaped bottom electrode and the interior of the recess.

BRIEF DESCRIPTION OF THE DRAWINGS

Features and advantages of the present invention will become more apparent from the following description of the preferred embodiments described below in detail with reference to the accompanying drawings where:

FIG. 1 is a top plan view of a portion of an in-process DRAM substrate assembly of the prior art.

FIG. 2 is a cross-sectional view of the in-process DRAM substrate assembly having undergone known processes in the art.

5 FIG. 3 is a cross-sectional view of the in-process DRAM substrate assembly having undergone alternative known processes in the art.

FIG. 4 is a partial top plan view illustrating an exemplary embodiment of the present invention as applied to an in-process DRAM substrate assembly.

10 FIG. 5 is a cross-sectional view of an in-process DRAM substrate assembly of the prior art.

FIG. 6 is a cross-sectional view of the in-process DRAM substrate assembly having undergone at least one additional process known in the art.

FIG. 7A is a cross-sectional view along B-B of FIG. 4 illustrating steps in a first exemplary embodiment of the present invention.

15 FIG. 7B is a cross-sectional view along B-B of FIG. 4 illustrating alternate steps in a second exemplary embodiment of the present invention.

FIG. 7C is a three-dimensional view indicating additional steps taken in accordance with an exemplary embodiment of the current invention.

20 FIG. 8A is a cross-sectional view of the in-process DRAM substrate assembly having undergone additional processing under an exemplary embodiment of the current invention.

FIG. 8B is a three-dimensional view of the in-process DRAM substrate assembly having undergone exemplary steps within the scope of the current invention.

FIG. 9A is a cross-sectional view of an in-process DRAM substrate assembly having undergone still more processing according to an exemplary embodiment of the current invention.

FIG. 9B is a three-dimensional view of the in-process DRAM substrate assembly
5 having undergone additional exemplary steps within the scope of the current invention.

FIG. 10A is a cross-sectional view of an in-process DRAM substrate assembly illustrating yet more processing according to an exemplary embodiment of the current invention.

FIG. 10B is a three-dimensional view of an in-process DRAM substrate assembly
10 having undergone exemplary steps within the scope of the current invention.

FIG. 11A is a cross-sectional view of an in-process DRAM substrate assembly after even more steps covered by an exemplary embodiment of the current invention.

FIG. 11B is a three-dimensional view of an in-process DRAM substrate assembly having undergone exemplary steps within the scope of the current invention.

FIG. 12 is a cross-sectional view along C-C of the in-process DRAM substrate
15 assembly with bit lines.

FIG. 13 is a cross-sectional view of an alternative exemplary apparatus embodiment of the current invention that also illustrates the steps to be taken in an exemplary process embodiment of the current invention.

FIGs. 14A-F are cross-sectional views of yet another alternative exemplary
20 embodiment of the current invention.

FIGs. 15A-G are cross-sectional views of still another alternative exemplary embodiment of the current invention.

FIGs. 16A-G are cross-sectional views of another alternative exemplary embodiment of the current invention.

FIGs. 17A-G are cross-sectional views of another alternative exemplary embodiment of the current invention.

5 FIGs. 18A-G are cross-sectional views of another alternative exemplary embodiment of the current invention.

Reference numbers refer to the same or similar parts of embodiments of the present invention throughout the several figures of the drawing.

10 DESCRIPTION OF THE PREFERRED EMBODIMENTS

In the following detailed Description of the Preferred Embodiments section, reference is made to the accompanying drawings which form a part of this disclosure, and which, by way of illustration, are provided for facilitating understanding of the specific embodiments. It is to be understood that embodiments, other than the specific
15 embodiments disclosed herein, may be practiced without departing from the scope of the present invention. The following exemplary embodiments, directed to manufacture of dynamic random access memories (DRAMs), are provided to facilitate understanding of the present invention. Accordingly, some conventional details with respect to manufacture of DRAMs have been omitted to more clearly describe the exemplary
20 embodiments herein.

FIG. 4 is a top plan view of an in-process substrate assembly 10C forming a portion of a memory array and serving as one exemplary embodiment of the current invention. Recesses 3 are formed in dielectric 19 and expose exterior surface portions 4 of

exterior surface 9 of in-process container capacitor structures 8C. Accordingly, recesses 3 between adjacent container capacitors are available for depositing dielectric layer 23C and conductive layer 24C (shown in FIGs. 8A and B) on exterior surface portions 4, thereby allowing for additional capacitance. Other portions of exterior surface 9 of in-process container capacitor structures 8C are in contact with dielectric layer 19. Hence, deposition of dielectric layer 23C and conductive layer 24C does not reach the exterior surface 9 at those portions. As a result, adequate spacing between container capacitors and contacts is maintained.

The stage of the in-process substrate assembly 10C achieved in FIG. 4 is reached through steps depicted in the subsequent figures. Referring to FIG. 5, there is shown a cross-sectional view of an exemplary portion of an embodiment of an in-process DRAM substrate assembly 10 of the prior art. Substrate 11 is a slice of single crystalline silicon. Conventionally, as a DRAM memory array uses NMOSFETs (n-channel metal-oxide-semiconductor field effect transistors), a P-well 12 is formed in substrate 11. Moreover, substrate 11 may have P-type impurities (e.g., boron) added thereto. Though NMOSFETs are described herein, it should be understood that alternatively P-channel MOSFETs may be used. Isolation regions 13 provide isolation from adjacent pairs of memory cells, such regions may be field oxides or shallow trench isolations (STIs). STI regions 13 may be formed in substrate 11 and filled with a combination of a thermal oxide and a high-density plasma (HDP) oxide.

N-type source, drain and contact regions 14A, 14B and 14C, formed in P-well 12, are for transistor stacks 16 and for electrical contact to conductive studs 15. N-type regions 14A, 14B and 14C may include lightly doped drains (LDDs). Conductive studs

15 may comprise polycrystalline silicon ("polysilicon") having N-type impurities (e.g., phosphorous and/or arsenic) added thereto, for conductivity; however, other conductive materials may be used.

Transistor stacks 16 are formed over substrate 11. Each transistor stack 16 may
5 comprise gate dielectric 40 (e.g., a thermal oxide), gate conductors 41 and 42 (e.g., a conductive polysilicon under tungsten silicide), dielectric anti-reflective coating (DARC) 43 (e.g., a nitride), and dielectric cap 44 (e.g., a nitride). One or both of gate conductors 41 and 42 may be used as a row line in a memory array. Spacer layer 17 is illustratively shown as covering transistor gate stack 16; however, spacer layer 17 may be etched or
10 otherwise removed such that it is not disposed above dielectric cap 44.

Dielectric layers 18 and 19 are separate layers, which may be made of the same or different materials. By way of example and not limitation, a silicon oxide having impurities ("dopants") added thereto may be used for dielectric layers 18 and 19. Moreover impurities such as phosphorous and boron may be used to enhance flow
15 characteristics for deposition of dielectric layers 18 and 19. Accordingly, dielectric layers 18 and 19 may comprise boro-phospho-silicate glass (BPSG) or phospho-silicate glass (PSG). Alternatively, other low dielectric constant materials may be used including but not limited to other oxides, especially porous oxides.

Conductive layer 20, which may comprise one or more layers of one or more
20 materials, forms a cup-shaped bottom electrode of each container capacitor structure. Notably, by cup-shaped bottom electrode, it should be understood to include any of circular, square, rectangular, trapezoidal, triangular, oval, or rhomboidal, among other shapes, with respect to the top down view of bottom electrodes shown in FIG. 4.

Conventionally, conductive layer 20 is formed of N-type hemispherical grain silicon (HSG). However, a P-type material may be used. Accordingly, impurities such as boron, phosphorous and/or arsenic may be used. Moreover, a conductively formed polysilicon, ruthenium, ruthenium oxide, or like material may be used for conductive layer 20. A
5 flow-fill material 21, such as photosensitive polymer ("photoresist"), is provided within the capacitor structures 8 and cured.

Referring to FIG. 6, there is shown a cross-sectional view of substrate assembly 10 of FIG. 5 after a planarization step separating the bottom electrodes.

FIG. 7A illustrates that etch mask 27 is then deposited and patterned. Etch mask
10 27 may comprise a photosensitive polymer. Alternatively, as illustratively shown in the cross-sectional view of FIG. 7B, flow-fill material 21 may be removed prior to depositing etch mask 27. In addition, FIG. 7B shows that etch mask 27 may extend to exterior surface portions 4. However, it may be difficult from a lithography standpoint to precisely align the edges of etch mask 27 with the exterior surface portions 4. Misalignment may
15 result in the etch mask 27 being shifted to one side so that it extends past an exterior surface portion 4. As a result, the etch 28 would not expose the conductive layer 20 underlying that extension, and subsequent steps may not achieve the additional capacitance desired. Therefore, to ease lithographic tolerances, the etch mask 27 can be made to extend only within the boundary of the exterior surface portions 4, as exemplified
20 by dashed lines 50. Also to ease the lithography, dielectric layer 19 should be planar (within plus or minus 50 nm (500 angstroms)) with upper surface 6 of conductive layer 20 of in-process container capacitor structures 8C. Thus, assuming that a "stacked" capacitor (such as the one disclosed in figure 1 of United States Patent Number

5,145,801) could be considered to be “cup-shaped,” the planarity of upper surface 6 distinguishes the current embodiment from such a configuration.

With continuing reference to FIG. 7A, a portion of dielectric layer 19 is removed by etch 28. Dielectric layer 19 may be removed to some level above, down to, or into dielectric layer 18. By way of example (and not limitation), it is assumed that dielectric layer 19 is BPSG and is to be etched down to a level above another BPSG dielectric layer 18. In such an embodiment, a silicon oxide etch selective to the polysilicon forming conductive layer 20 may be used. If dielectric layer 19 is removed down to or into dielectric layer 18, it may be advantageous to form dielectric layers 18 and 19 of different materials for purposes of etch selectivity. Moreover, if dielectric layer 19 removal involves etching into dielectric layer 18, it is understood that the etching process should selectively etch dielectric layers 18 and 19 rather than the material forming cap 44 and/or spacer 17.

Regardless of whether masking occurs as illustrated in FIG. 7A or 7B, once the etch mask 27 is removed, the substrate assembly 10C appears as illustrated in FIG. 7C. This figure depicts a portion of the DRAM substrate assembly 10C of FIG. 4 but from a different perspective and with emphasis on the contact sites 5 along or near axis C-C. Each contact site 5 is surrounded by a discrete portion of dielectric layer 19. As this portion of dielectric layer 19 not only encompasses the contact site 5 but also extends beyond the site to the neighboring conductive layers 20, the dielectric could be described as “over-encompassing” the contact site 5. Of special note are the areas of the electrodes that face a contact site 5 and hence abut the dielectric layer 19. For example, areas 102, 104, and 106 of electrode 100 face contact sites 5, 5', and 5'' and contact dielectric layer

19 accordingly. Areas of electrode 100 that are askew or face away from a contact site 5 are distal from and do not contact dielectric layer 19. More specifically, such areas face another electrode through the recesses 3 formed in dielectric layer 19. For example, dielectric layer 19 has been recessed from between electrode 100 and electrode 108, electrode 100 and electrode 110, and electrode 100 and electrode 112.

Preferably, the areas 102, 104 or 106 abutting the dielectric layer 19 represent no more than 50% of the total exterior vertical surface area of the relevant bottom plate. More preferably, areas such as 102, 104 or 106 represent no more than 20% of a given plate's total exterior vertical surface area. Alternatively, it could be expressed that etch 28 preferably exposes at least 50% of the total exterior vertical surface area of the bottom plate, and even more preferably exposes at least 80%. These preferences could also be expressed in terms of the circumference defined by the exterior of the cup-shaped capacitor electrode. Thus, it is preferred that dielectric layer 19 abut no more than 50% of that circumference, and it is even more preferred that dielectric layer 19 remain separate from at least 50% (and more preferably 80%) of that circumference.

One skilled in the art can now appreciate that, when a dielectric and top electrode are subsequently deposited, those layers will not deposit between a bottom electrode and its neighboring contact site 5 because of the presence of dielectric layer 19. However, the layers will deposit within the recesses 3 and thereby add to the capacitance of all capacitors sharing those layers. FIG. 8A illustrates such depositions. FIG. 8A shows that, after etch mask 27 is removed, capacitor dielectric 23C is formed. Capacitor dielectric 23C is formed of one or more layers and/or materials. Capacitor dielectric 23C may be a nitride film; however, a tantalum oxide may be used. A nitride film equal to or less than 6

nm (60 angstroms) thick may be deposited followed by exposure to a dry or a wet oxygenated environment to seal it. In this embodiment with a nitride film equal to or less than 6 nm thick, oxygen may diffuse through it causing a silicon dioxide to form underneath. Accordingly, an oxide-nitride-oxide (ONO) thin film dielectric may be
5 formed.

After forming capacitor dielectric 23C, conductive layer 24C is formed to provide a second electrode of each container capacitor structure. This electrode is sometimes referred to as a "top electrode" or cell plate. Conductive layer 24C may comprise one or more layers of one or more materials. A polysilicon, with N-type or P-type impurities
10 added thereto for conductivity, may be used. However, a platinum, ruthenium, or ruthenium oxide-like material (including other conductive oxides) may be used. Notably, if a conductive nitride or oxide is used, a barrier material (not shown) may be inserted between conductive layer 20 and the conductive stud 15 to prevent oxidation.

Of further note in FIG. 8A is that, for a particular capacitor, there are at least two
15 elevations within the substrate assembly 10C at which the dielectric 23C or conductive material 24C extends away from the conductive layer 20. In region 1, facing the contact site 5, the dielectric 23C and conductive material 24C extend away from the conductive material 20 and toward the contact site 5 at a level near the top of dielectric 19 or the top of the conductive material 20. At region 2, however, the dielectric 23C and conductive
20 material 24C extend away from the conductive material 20 and away from the contact site 5 at a level near the bottom of dielectric 19.

An alternative way of describing the configuration in FIG 8A involves referring to a material next to but not included as part of the capacitor -- perhaps a material supporting

the capacitor structure. In FIG. 8A, such a material could include dielectric 19 (and dielectric 18 as well). FIG. 8A reveals that the capacitor dielectric 23C, conductive layer 20, and dielectric support material 19/18 meet at different levels. In region 1, capacitor dielectric 23C, conductive layer 20, and dielectric 19 meet at a level commensurate with the top of conductive layer 20; whereas in region 2, capacitor dielectric 23C, conductive layer 20, and dielectric 18 meet at a lower level. Regardless of the particular elevations, an exemplary difference in elevations of these levels is at least 500 angstroms. More specific differences in elevations include ones of at least 1000 or 2000 angstroms.

Subsequent steps are also addressed in FIG. 8A and beyond. After formation of conductive layer 24C, etch mask 29 is deposited and patterned. Etch mask 29 may comprise a photosensitive polymer. Etch 30 is used to remove portions of conductive layer 24C and capacitor dielectric layer 23C. However, etch 30 need not remove capacitor dielectric layer 23C at this stage, as it is not required to expose underlying dielectric layer 19 at this point in the process.

FIG. 8B offers another perspective. FIG. 8B shows that, initially after deposition yet before masking and etching, conductive layer 24C blankets the in-process substrate assembly 10C. In doing so, conductive layer 24C inhabits the interior of the bottom electrodes as well as the interior of the recesses 3. Moreover, in this embodiment, the deposition of the conductive layer 24C is commensurate with the extent of deposition of the underlying capacitor dielectric layer 23C.

FIG. 9A illustrates the subsequent removal by etch 30 of a portion of conductive layer 24C and capacitor dielectric layer 23C. It should be noted that the opening 45 caused by etch 30 is wider than the contact site 5. By having a wider opening 45,

capacitor dielectric layer 23C and conductive layer 24C are removed farther away from contact site 5 as compared to a narrower contact etch that may be practiced in the prior art assembly of FIG. 2. Figure 9A shows that this embodiment allows for portions of capacitor dielectric layer 23C and conductive layer 24C to be removed at a relatively high level with respect to the bottom of the contact site 5. As discussed previously, this allows for easier and more effective removal. Moreover, etch 30 may be used to undercut etch mask 29 as illustratively indicated by dashed-lines 31. FIG 9B offers another perspective of the substrate assembly 10C after etch mask 29 has been removed.

Referring to FIG. 10A, there is shown a cross-sectional view of substrate assembly 10C after dielectric layer 33, which may comprise a silicon oxide such as PSG or BPSG, is deposited. After depositing dielectric layer 33, etch mask 34 is deposited and patterned. Etch mask 34 may comprise a photosensitive polymer. Etch 35 forms contact via 32 by removing portions of dielectric layer 33 and dielectric layer 19, thereby exposing conductive stud 15 above N-type region 14B. Notably, if a portion of capacitor dielectric layer 23C is not previously removed to expose underlying dielectric layer 19, then etch 35 may be used to remove that portion. FIG. 10B shows a three-dimensional viewpoint of this stage, with the dielectric layer 33 and etch mask 34 not shown for the sake of clarity.

Referring to FIG. 11A, there is shown a cross-sectional view of substrate assembly 10C after removing etch mask 34. Conductive layer 36 is subsequently deposited and at least partially fills the contact via 32 identified in FIG. 10A. If conductive layer 36 forms over dielectric layer 33, it may be subjected to CMP or etch back, as in a damascene process, or patterned and etched, as in a photo/metal etch process. Accordingly, contact plug 37 and contact stud 15 in combination provide a contact for electrical connection to

region 14B for accessing transistors on either side thereof. Figure 11B offers the three-dimensional perspective, with dielectric layer 33 once again removed for clarity's sake.

As a result, the capacitors are configured to allow for capacitance using a portion of a particular bottom electrode's exterior surface 9 that is askew from a plug 37, while
5 another portion of the exterior surface 9 facing a plug 37 is not used for capacitance.

Referring to FIG. 12, there is shown a cross-sectional view of substrate assembly 10C along C-C of FIG. 4 after forming bit lines 38.

A container capacitor structure of the present invention is particularly well-suited for high-density memory array architectures. In one exemplary embodiment, the container
10 capacitor structure may have a bottom electrode with a maximum interior width equal to or less than 0.15 microns and/or a maximum exterior width equal to or less than 0.35 microns. Such a high-density memory array architecture may have adjacent bit lines 38 (shown in FIG. 12) with a pitch equal to or less than 0.40 microns. Though a bit line over contact formation is described herein, it should be understood that buried bit line
15 architecture may be used as well. In a high-density memory array, critical dimension (CD) of a contact may be equal to or less than 0.32 microns wide, and word line-to-word line pitch in such an array may be equal to or less than 0.40 microns.

The above-discussed exemplary embodiments of the present invention provide a container capacitor structure and process of constructing it. Such a container capacitor
20 structure provides increased capacitance without having to clear a portion of a capacitor top electrode from a bottom of a contact via. Moreover, such a container capacitor structure provides space between a contact plug and a capacitor top electrode such that probability of shorting therebetween is not increased.

While the above-described embodiments of the present invention were directed to DRAM manufacture, the present invention may be implemented in a variety of other integrated circuit devices (memory devices, logic devices having embedded memory, application specific integrated circuits, microprocessors, microcontrollers, digital signal
5 processors, and the like incorporating a memory array) which employ one or more container capacitors. Moreover, a memory or a memory module having a container capacitor formed in accordance with the present invention may be employed in various types of information handling systems (network cards, telephones, scanners, facsimile machines, routers, televisions, video cassette recorders, copy machines, displays, printers,
10 calculators, and personal computers, and the like incorporating memory). In addition, the current invention is not limited to container capacitors. Also included within the scope are other non-planar devices or devices having a component that is vertical with respect to the underlying support surface. FIG. 13, for example, illustrates a substrate assembly 10D including stud capacitors rather than container capacitors, wherein studs 200 are made of a
15 conductive material and serve as bottom electrodes. The portions of studs 200 facing the contact plug 37 are free of conductive layer 24C. This can be achieved using methods such as the ones described above for a container capacitor.

Moreover, alternative methods that fall within the scope of the current embodiment may be used to provide partial double-sided capacitance. For example, processing may
20 proceed as described above to achieve the structure depicted in FIG. 6. Rather than depositing and patterning etch mask 27 at that point (shown in FIG. 7A), another alternative (shown in FIG. 14A) is to layer an oxide 300 over dielectric layer 19 (and the tops of conductive layer 20). Preferably, this oxide 300 is provided using a low

temperature process, such as a plasma deposition with tetraethylorthosilicate (TEOS) as a precursor, as is known in the art. The oxide is subsequently patterned (FIG. 14B) so that it covers at least portions of dielectric 19 that are between a conductive layer 20 and a contact site 5. As seen in FIG. 14C, a subsequent dry etch removes uncovered portions of dielectric 19 (thereby forming recesses 3) and flow-fill material 21. Optionally, the in-process device may also be subjected to a wet dip at this stage. FIG. 14D shows that capacitor dielectric 23C and conductive layer 24C are then deposited over conductive layer 20 and oxide 300. In doing so, the capacitor dielectric 23C and conductive layer 24C at least line if not completely fill the recesses 3 and interiors of the cup-shaped bottom capacitor plates. Next, as seen in FIG. 14E, the surface is planarized down to the oxide 300 using, for example, CMP. Subsequent steps, such as those described above, may then be used to clear at least a portion of oxide 300 from above the contact site 5, and to form and fill the via at the contact site 5. This method helps to further ensure that the conductive layer 24C does not encroach too closely to the contact site 5. Preferably, the patterned oxide 300 is aligned with the remaining portions of dielectric 19 as depicted in FIG. 14B and again in three-dimensions in FIG. 14F. However, alignment of the patterned oxide 300 over contact site 5 and the surrounding dielectric 19 may be somewhat challenging to accomplish.

Thus, an alternative embodiment helpful in keeping the conductive layer 24C from the contact site 5 is illustrated in Figures 15A-F. Figure 15A is similar to Figure 6, with the stipulation that conductive layer 20 and dielectric 19 extend vertically enough to account for a subsequent etchback of conductive layer 20 using techniques known in the art. Accordingly, this etchback is performed, and Figure 15B illustrates the result. Figure

15C demonstrates that photoresist 400 is subsequently deposited and patterned to cover the contact site 5 and its surrounding dielectric 19. A dry etch is then performed, removing portions of the dielectric that are distal from a contact site -- thereby forming the recesses 3 pictured in Figure 15D and addressed in previous embodiments. This dry etch also clears at least a portion of the interior of the container shape defined by conductive layer 20. However, it is possible that the patterned photoresist 400 will extend over that interior, in which case some amount of flow-fill 21 will remain despite the dry etch. This can be seen in FIGs. 15D and 15E. A wet etch can be performed to remove the remaining flow-fill 21, and the result of such an etch is seen in Figure 15F. Figure 15G indicates that the next step is to remove the photoresist 400, thereby leaving a portion of dielectric 19 extending higher than the conductive layer 20. Subsequent steps track those seen in Figures 14D, 14E, and the relevant text: the capacitor dielectric 23C and conductive layer 24C are deposited, and a CMP step removes at least the conductive layer 24C from over the contact site 5 and surrounding dielectric 19. It is preferable that the etchback in illustrated in Figure 15B be sufficient to ensure that the CMP step does not remove other portions of the conductive layer 24C needed to generate capacitance.

Moreover, this process of ensuring adequate spacing between conductive layer 24C and contact sites 5 is not limited to container capacitors. Figures 16A-G demonstrate that the process works on other vertical capacitors as well. These figures specifically illustrate the construction of a memory device incorporating stud capacitors similar to those discussed above in connection with Figure 13. Figure 16A illustrates that studs 200 serve as the bottom electrode for the in-process capacitors. These studs are recessed, as seen in Figure 16B, by etching methods known in the art. Photoresist 400 is deposited and

patterned, thereby covering the contact site 5 and the portion of dielectric 19 surrounding that site 5 (Figure 16C). As in the previous embodiment, photoresist 400 is allowed to extend laterally beyond that portion of dielectric 19. Thus, in the event that the patterned photoresist 400 is misaligned with respect to the underlying dielectric 19, it is less likely that dielectric 19 will be exposed to the subsequent etch. Accordingly, a dry etch is then performed to form recesses 3 seen in Figure 16D. Unlike the previous embodiment, the extension of patterned photoresist 400 does not require an additional wet etch, as extended portions of photoresist 400 merely cover the studs 200. The photoresist 400 is then removed (Figure 16E) and capacitor dielectric 23C is deposited, followed by conductive layer 24C (Figure 16F). It should be noted that, in this exemplary embodiment, the thickness of conductive layer 24C and the dimensions of the recesses 3 are such that conductive layer 24C fills rather than merely lines the recesses 3. Such a result may be provided for in any other exemplary embodiment discussed herein as well as others within the scope of the current invention. A CMP step achieves the state of the substrate assembly depicted in Figure 16G, and further processing may proceed as discussed in previous exemplary embodiments.

In addition, it should be noted that the last few embodiments described above involve two planarization steps: one to planarize conductive layer 20 (see, for example, FIG. 6), and another to planarize capacitor dielectric 23C and conductive layer 24C (FIGs. 14E, 16G). However, the current invention includes within its scope embodiments that have fewer planarization steps. One such exemplary embodiment appears in FIGs. 17A-17G. In FIG. 17A, conductive layer 20 has been deposited over dielectric 19. Rather than planarize conductive layer 20, FIG. 17B demonstrates that a photoresist layer 500 is

deposited thereover. Subsequent patterning of photoresist layer 500 results in the substrate assembly depicted in FIG. 17C, wherein developed photoresist 500 covers the portion of the dielectric 19 that encompasses the contact site 5 and extends to conductive layer 20's vertical surfaces. Further, undeveloped photoresist 500' remains at the bottom of the container capacitor structures 8D. A subsequent anisotropic etch removes portions of the conductive layer 20 outside of the container capacitor structures 8D and recesses the conductive layer 20 within the container capacitor structures 8D; the result of this etch is seen in FIG. 17D. That figure also illustrates that the undeveloped photoresist 500' prevents the anisotropic etch from removing the conductive layer 20 from the bottom of the container capacitor structures 8D. However, even if there were no photoresist at the bottom of the container capacitor structures 8D, etching of the conductive layer 20 at the bottom is not necessarily detrimental, as doing so merely exposes another conductive material -- the underlying conductive stud 15. The conductive material of stud 15 can serve as a part of the bottom plate in the event the overlying portion of conductive layer 20 is removed. It should be further noted that a container capacitor structure 8D can be tapered -- becoming narrower closer to the bottom -- to ensure the continuity of conductive material for the bottom plate. An anisotropic oxide etch is then performed to define the recesses 3 (FIG. 17E). Next, the photoresist 500, 500' is removed, and capacitor dielectric 23C and conductive layer 24C are deposited, as seen in FIG. 17F. A following CMP step removes portions of conductive layer 24C, capacitor dielectric 23C, and conductive layer 20 that overlie the contact site 5; and the result is depicted in FIG. 17G.

In the event that it is difficult to align the hardened photoresist 500 with the contact site 5 and dielectric 19 as depicted in FIG. 17C, then an alternative embodiment pictured in FIGs. 18A-18G may be pursued. After depositing photoresist 500 as seen in FIG. 17B, subsequent patterning results in the substrate assembly of FIG. 18A. In that figure, photoresist 500 is wider than the portion of dielectric 19 encompassing the contact site 5 and extending to the vertical surfaces of conductive layer 20. This helps to ensure coverage of this portion of dielectric 19 in the event of a misaligned pattern. As a result, photoresist may extend into the container capacitor structures 8E and cover parts of conductive layer 20 that face the contact site 5. Accordingly, the subsequent anisotropic etch (preferably a dry etch) of the conductive layer 20 will not affect those parts. Nevertheless, the etch will still remove portions of the conductive layer 20 outside of the container capacitor structures 8E and recess some the conductive layer 20 within the container capacitor structures 8D. The result of this etch is seen in FIG. 18B. In order to recess the remaining portion of conductive layer 20 within the container capacitor structures 8D, an isotropic etch, either dry or wet, is used. The result is pictured in FIG. 18C, wherein the conductive layer 20 is recessed along the entire circumference of the container capacitor structures 8E, leaving gaps 502 between the conductive layer 20, dielectric 19, and photoresist 500. What follows is an oxide etch defining the recesses 3 (FIG. 18D); removal of photoresist 500 (FIG. 18E); deposition of capacitor dielectric 23C and conductive layer 24C (FIG. 18F); and CMP of portions of conductive layer 24C, capacitor dielectric 23C, and conductive layer 20 that overlie the contact site 5 (FIG. 18G). Processing may then continue as described in previous exemplary embodiments.

The present invention has shown and described with respect to certain preferred embodiments. However, it will be readily appreciated to those of ordinary skill in the art that a wide variety of alternate embodiments, adaptations or variations of the preferred embodiments, and/or equivalent embodiments may be made without departing from the intended scope of the present invention as set forth in the appended claims. For instance, the current invention would generally apply to any circuit having a first device defining an axis and a second device with one side near the first device and another side far from the device. The second device would include an element that defines a plurality of layers at the far side and less than that plurality of layers on the near side, wherein the layers extend along the axis defined by the first circuit device. The current invention also includes methods for making the device described above. More specifically, the devices and methods of the current invention may be applied to metal-insulator-metal capacitors. Accordingly, the present invention is not limited except as by the claims.

CLAIMS

What is claimed is:

1. A capacitor within a substrate assembly, comprising:

a first electrode having a container shape defining a planar top surface;

a dielectric over said first electrode; and

a second electrode over said dielectric and extending from said container shape at
at least two different levels within said substrate assembly.

2. The capacitor in claim 1, wherein said second electrode extends from said container
shape at a first level and at a second level, and wherein said first level and said second
level define a difference in height of at least 500 angstroms.

3. The capacitor in claim 2, wherein said first level and said second level define a
difference in height of at least 1000 angstroms.

4. The capacitor in claim 3, wherein said first level and said second level define a
difference in height of at least 2000 angstroms.

5. The capacitor in claim 1, wherein said second electrode comprises:

a first portion extending from said container shape at a first level lower than a top
of said container shape; and

a second portion extending from said container shape at a second level higher than
said first level.

6. The capacitor in claim 1, wherein said second electrode comprises:

a first portion extending from said container shape at a first level at least as high as

a top of said container shape; and

5 a second portion extending from said container shape at a second level lower than
said first level.

7. The capacitor in claim 6, wherein said dielectric extends from said container shape
under said first and second portion of said second electrode.

10 8. A storage device environment, comprising:

a first plate defining a uniform vertical length;

at least one material external to said first plate;

a capacitor dielectric contacting said first plate, wherein:

15 said first plate, a first portion of said at least one material, and said

capacitor dielectric meet at a first elevation along said vertical
length; and

said first plate, a second portion of said at least one material, and said

capacitor dielectric meet at a second elevation along said vertical

20 length; and

a second plate contacting said capacitor dielectric.

9. The storage device environment in claim 8, wherein said second plate and said

capacitor dielectric are coextensive.

10. The storage device environment in claim 8, wherein said first portion of said at least one material is from a first material; and wherein said second portion of said at least one material is a from a second material.

11. The storage device environment in claim 10, wherein said first material and said second material are dielectric.

12. The storage device environment in claim 11, wherein said first portion of said at least one material encompasses a contact site.

13. An array of capacitors, comprising:

a first bottom capacitor plate;

a second bottom capacitor plate;

a third bottom capacitor plate;

a contact between said first bottom capacitor plate and said second bottom capacitor plate;

a trench between said second bottom capacitor plate and said third bottom capacitor plate;

a common top capacitor plate over said first bottom capacitor plate, said second bottom capacitor plate, and said third bottom capacitor plate, wherein said top capacitor plate extends toward said contact at a first level within said

array and is separate from said contact, and wherein said top capacitor plate
lines a side of said trench and further lines a bottom of said trench at a
second level within said array; and
a dielectric between said top capacitor plate and said first, second, and third bottom
5 capacitor plates.

14. The array in claim 13, wherein said top capacitor plate extends toward a top of said
contact.

10 15. A container capacitor structure, comprising:
a cup-shaped electrode having an interior surface and an exterior surface, wherein
said exterior surface comprises a first portion and a second portion coextensive
in height with said first portion;
an insulating layer contacting the exterior surface on the first portion;
15 a dielectric layer disposed on the interior surface and on the exterior surface on said
second portion; and
a conductor layer disposed on the dielectric layer.

16. The container capacitor structure of claim 15, wherein the cup-shaped electrode
20 comprises hemispherical-grain-silicon.

17. The container capacitor structure of claim 15, wherein the cup-shaped electrode
has an interior width of no greater than 200 nm.

18. The container capacitor structure of claim 15, wherein the cup-shaped electrode has an exterior width of no greater than 300 nm.

5 19. A portion of a memory array having memory cells operatively coupled to row lines and column lines, the portion of the memory array comprising:

a plurality of contacts;

a plurality of container capacitors proximal to the contacts, each of the container

capacitors having a bottom electrode, a dielectric, and a top electrode;

10 wherein each bottom electrode has a cup-shape; wherein the dielectric is disposed on and in each container capacitor and further disposed between at least one pair of bottom electrodes of the plurality of container

capacitors; and wherein the top electrode is disposed on the dielectric, in each container capacitor, and between the at least one pair of bottom

15 electrodes; and

an insulating layer disposed between the contacts and bottom electrodes.

20. The portion of the memory array of claim 19, wherein the column lines are on a pitch of no greater than 0.5 microns.

21. The portion of the memory array of claim 20, wherein each of the contacts is surrounded by six of the container capacitors.

22. The portion of the memory array of claim 21, wherein each of the contacts has a critical dimension of no greater than 0.32 microns.

23. In a dynamic random access memory array, at least a portion of the memory array
5 comprising:

a plurality of bit lines;

a plurality of contacts operatively coupled to the bit lines;

a plurality of memory cells operatively coupled to the contacts, each of the
memory cells having a container capacitor, the memory cells arranged such that container
10 capacitors are disposed around a contact;

container capacitor bottom electrodes spaced apart from one another and spaced
apart from the contact;

container capacitor dielectric disposed between the container capacitor bottom
electrodes and not disposed between the contact and the container capacitor bottom
15 electrodes; and

a container capacitor top electrode disposed between the container capacitor
bottom electrodes and not disposed between the contact and the container capacitor
bottom electrodes.

20 24. The portion of the memory array of claim 23, wherein the bit lines are disposed
above the container capacitors.

25. The portion of the memory array of claim 24, wherein the bit lines are on a pitch of
no greater than 0.5 microns.

26. Container capacitor structures, comprising:

bottom electrodes having a cup-shape, the bottom electrodes having an interior surface and an exterior surface;

5 at least one insulating layer in contact with the exterior surface of the cup-shaped bottom electrodes and defining a recess between a first pair of cup-shaped bottom electrodes;

a dielectric layer disposed on the interior surface of the cup-shaped bottom electrodes and on the exterior surface between the first pair of the cup-shaped bottom electrodes; and

10 a top electrode layer on the dielectric layer opposite the interior surface of the cup-shaped bottom electrodes and opposite the exterior surface between the first pair of the cup-shaped bottom electrodes.

15 27. The container capacitor structures in claim 26, wherein said at least one insulating layer defines a contact site between a second pair of the cup-shaped bottom electrodes.

28. The container capacitor structures in claim 26, wherein the first pair of the cup-shaped bottom electrodes and the second pair of the cup-shaped bottom electrodes share a

20 common cup-shaped bottom electrode.

29. A method for forming a container capacitor, comprising the steps of:

providing a cup-shaped bottom electrode;

providing an insulating layer around an exterior surface of said cup-shaped bottom

electrode;

masking a first portion of said insulating layer;

etching a second portion of said insulating layer from a part of said exterior surface;

- 5 depositing a dielectric layer on said part of said exterior surface; and
 depositing a conductive layer on said dielectric layer.

30. A method for forming at least a portion of a memory array, comprising the steps of:

- 10 providing a substrate assembly;
 providing a plurality of cup-shaped electrodes on said substrate assembly;
 providing an insulating layer around exterior surfaces of said cup-shaped electrodes;
- 15 masking a portion of said insulating layer;
 etching recesses into said insulating layer in unmasked regions between the cup-shaped electrodes, said etching exposing portions of said exterior surfaces;
 depositing a dielectric layer on exposed portions of said exterior surfaces; and
 depositing a conductive layer on said dielectric layer.

- 20 31. A method for forming a portion of a memory array, comprising the steps of:
 providing a substrate assembly;
 providing an insulating layer on said substrate assembly, said insulating layer having holes formed therein;

providing a container capacitor bottom electrode in each of said holes of said
insulating layer;

masking a portion of said insulating layer and leaving mask gaps between adjacent
container capacitor bottom electrodes;

- 5 forming recesses in said insulating layer according to said mask gaps;
 depositing a dielectric into said recesses; and
 depositing a conductor on said dielectric and into said recesses.

32. A method for forming a portion of a memory array, comprising the steps of:

- 10 providing a substrate assembly;
 providing an insulating layer on said substrate assembly;
 forming holes in said insulating layer;
 forming a cup-shaped electrode in each of said holes;
 covering a portion of said insulating layer with a mask layer; and
15 etching recesses in unmasked portions of said insulating layer between adjacent
 cup-shaped electrodes.

33. A substrate assembly, comprising:

- a plug;
20 a first dielectric surrounding said plug; and
 a vertical capacitor structure comprising:
 a first electrode having:
 a first outer area facing said plug and contacting said first dielectric,

and

a second outer area facing away from said plug,

a second electrode conformal to said second outer area and excluded from

a region between said plug and said first outer area, and

5 a second dielectric between said first electrode and said second electrode.

34. The substrate assembly in claim 33, wherein said vertical capacitor structure is a stud capacitor.

10 35. A method of preparing a DRAM, comprising:

providing a first dielectric layer;

designating a plurality of contact sites within said first dielectric layer;

forming a plurality of first vertical capacitor electrodes in said first dielectric layer

and among said plurality of contact sites; and

15 defining a plurality of discrete portions of said first dielectric layer, wherein each

discrete portion extends from a contact site to first vertical capacitor

electrodes around said contact site.

36. The method in claim 35, further comprising:

20 providing a second dielectric layer over said plurality of first vertical capacitor

electrodes, over said plurality of discrete portions of said first dielectric

layer, and between said plurality of discrete portions of said first dielectric

layer;

providing a second vertical capacitor electrode over said second dielectric layer;
and
removing said second dielectric layer and said second vertical capacitor electrode
from areas extending over said plurality of contact sites and beyond.

5

37. A method of configuring a container capacitor including a bottom electrode,
comprising:

allowing for capacitance using a first portion of an exterior surface of said bottom
electrode, wherein said first portion is askew from a contact; and

10 allowing for capacitance without using a second portion of said exterior surface,
wherein said second portion faces said contact.

38. A circuit, comprising:

a first circuit device defining an axis; and

15 a second circuit device comprising:

a far side distal from said first circuit device,

a near side proximate said first circuit device, and

an element defining:

a plurality of layers at said far side, wherein each layer of said

20 plurality extends parallel to said axis, and

at least one layer at said near side and at most one layer less than

said plurality of layers, wherein said at least one layer

extends parallel to said axis.

39. The circuit in claim 38, wherein said near side is interposed between said far side and said first circuit device.

5 40. The circuit in claim 39, wherein said first circuit device is an electrically conductive device and said element is an electrically conductive element.

41. The circuit in claim 40, wherein said first circuit device is a conductive plug, said second circuit device is a capacitor, and said element is a capacitor electrode.

10

42. A fabrication method for an in-process substrate assembly including an insulator around a capacitor plate, wherein said insulator and said capacitor plate define a plane thereover, and said insulator includes a first portion contacting said plate and over-encompassing an opening site, said method comprising:

15

covering said first portion of said insulator with an oxide;
removing a part of said substrate assembly uncovered by said oxide, including
removing a second portion of said insulator contacting said capacitor plate
and free of an opening site;

layering a dielectric over said plate and over said oxide;

20

layering a conductive material over said dielectric; and
planarizing said conductive material down to said oxide.

43. The method in claim 42, further comprising a step of etching an opening within said opening site.

44. The method in claim 43, wherein said step of layering a dielectric over said plate
5 comprises layering a dielectric over a container-shaped plate.

45. The method in claim 44, wherein said step of layering a dielectric over a container-shaped plate comprises depositing said dielectric onto an interior of said container-shaped plate and a part of an exterior of said plate uncovered with said oxide.

46. The method in claim 45, wherein said step of removing a part of said substrate assembly comprises removing a flow-fill material from said interior of said container-shaped plate.

47. The method in claim 46, wherein said step of covering said first portion of said insulator with an oxide comprises:

layering said oxide onto said first portion of said insulator, said second portion of said insulator, and said plate; and
removing said oxide from said second portion of said insulator and said plate.

48. The method in claim 47, wherein said step of removing a part of said substrate assembly comprises:

plasma etching a portion of said substrate assembly; and

wet etching said portion of said substrate assembly.

49. A method of spacing a capacitor from a contact site, comprising:

providing insulation conformal to a first capacitor plate defining a container shape,

wherein a first part of said insulation incorporates said contact site and a

5 second part of said insulation is free of any contact site, and wherein said

first plate and said insulation extend to a common height;

providing additional insulation in an interior of said container shape;

reducing a height of said first plate;

providing an etch mask over said first part of said insulation;

10 allowing said etch mask to extend over said interior;

removing said second part of said insulation and said additional insulation;

removing said etch mask;

depositing a capacitor insulator over said first plate and said first part of said

insulation;

15 depositing a second plate over said capacitor insulator and over said first part of

said insulation; and

removing said second plate from over said first part of said insulation.

50. The method in claim 49, wherein said step of removing said second plate comprises

20 removing said second plate through chemical-mechanical planarization.

51. The method in claim 50, wherein said step of removing said second part of said

insulation and said additional insulation comprises:

dry etching said second part of said insulation and at least some of said additional insulation; and
wet etching a remaining amount of said additional insulation.

5 52. A memory cell, comprising:

a bottom plate of a capacitor having an exterior vertical surface, wherein said surface defines a circumference; and
insulation incorporating a contact site and abutting said exterior vertical surface at a first region and separate from said exterior vertical surface at a second region.

10 53. The memory cell of claim 52, wherein said first region represents no more than 50% of said circumference.

15 54. The memory cell of claim 53 wherein said second region represents at least 50% of said circumference.

55. A method of spacing a contact site from a plurality of conductive elements, comprising:

20 providing an insulation layer enveloping said contact site;
etching an opening in said insulation layer, said opening being spaced from said contact site;
providing a first conductive element within said opening, said first conductive

element reaching an elevation lower than a top of said insulation layer;
protecting a first region of said insulation layer from etching, said first region
including at least said contact site and an area extending from said contact
site to said first conductive element
5 excluding a second region of said insulation layer from etch protection, said
second region extending from said first conductive element and excluding
any contact site;
etching said second region of said insulation layer;
providing a second conductive element over said first conductive element and
10 over said first region of said insulation layer; and
removing a portion of said second conductive element over said first region of said
insulation layer.

56. The method in claim 55, wherein said step of providing a first conductive element
15 comprises:

providing a first conductive element reaching said top of said insulation layer; and
recessing said first conductive element.

57. The method in claim 56, wherein said step of providing a first conductive element
20 comprises providing a conductive stud.

58. The method in claim 57, wherein said step of protecting a first region of said
insulation layer comprises protecting a first region extending over said stud.

59. The method in claim 58 further comprising a step of providing a dielectric between said first conductive element and said second conductive element.

5 60. The method in claim 59, wherein:

said step of etching said second region of said insulation layer comprises etching a trench next to said first conductive element;

said step of providing a dielectric between said first conductive element and said second conductive element comprises lining said trench; and

10 said step of providing a second conductive element comprises filling said trench.

61. A method of providing double-sided capacitance and maintaining a distance between a capacitor and a contact site in a memory device, comprising:

encompassing said contact site within an insulation layer;

15 defining a container within said insulation layer, wherein said container is spaced from said contact site;

depositing a first conductive layer over said insulation layer, including depositing within said container and over said contact site;

20 removing a first part of said first conductive layer, wherein said first part is outside of said container;

recessing a second part of said first conductive layer, wherein said second part is inside of said container;

retaining a third part of said first conductive layer, wherein said third part is

outside of said container and over said contact site;
defining a recess in said insulation layer extending from said container and
extending away from said contact site;
depositing a capacitor dielectric within said recess and over said second and third
5 part of said first conductive layer;
depositing a second conductive layer over said capacitor dielectric; and
planarizing said second conductive layer, said capacitor dielectric, and said third
part of said first conductive layer down to said insulation layer.

10 62. The method in claim 61, further comprising:

depositing photoresist over said first conductive layer;
patterning said photoresist before said removing and recessing steps;
guiding said removing and recessing steps with said photoresist; and
removing said photoresist before said step of depositing a capacitor dielectric.

15

63. The method in claim 62, wherein said step of patterning said photoresist comprises
developing a portion of said photoresist over said contact site and over a portion of said
insulation layer, said portion of said insulation layer extending from said contact site to
said container, and wherein said portion of said photoresist is coextensive with said
20 portion of said insulation layer.

64. The method in claim 63, further comprising allowing undeveloped photoresist to
remain in said container during said removing and recessing steps.

65. The method in claim 62, wherein said step of patterning said photoresist comprises developing a portion of said photoresist over said contact site and over a portion of said insulation layer, said portion of said insulation layer extending from said contact site to
5 said container, and wherein said portion of said photoresist extends beyond said portion of said insulation layer.

66. The method in claim 65, wherein said step of recessing a second part of said first conductive layer comprises:

10 anisotropically etching a first region of said second part uncovered by said photoresist; and
isotropically etching a second region of said second part covered by said photoresist.



FIG. 1
(PRIOR ART)

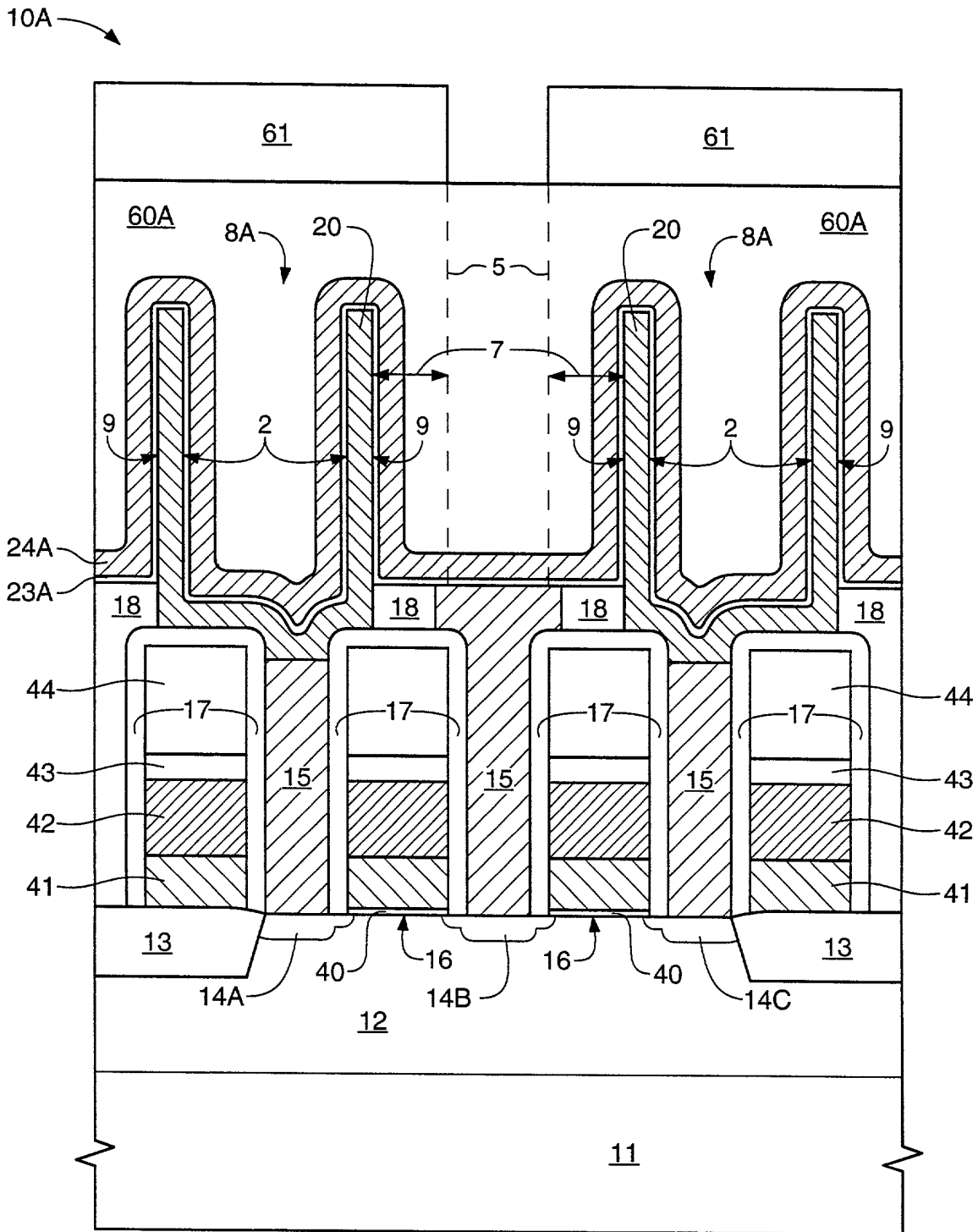


FIG. 2
(PRIOR ART)

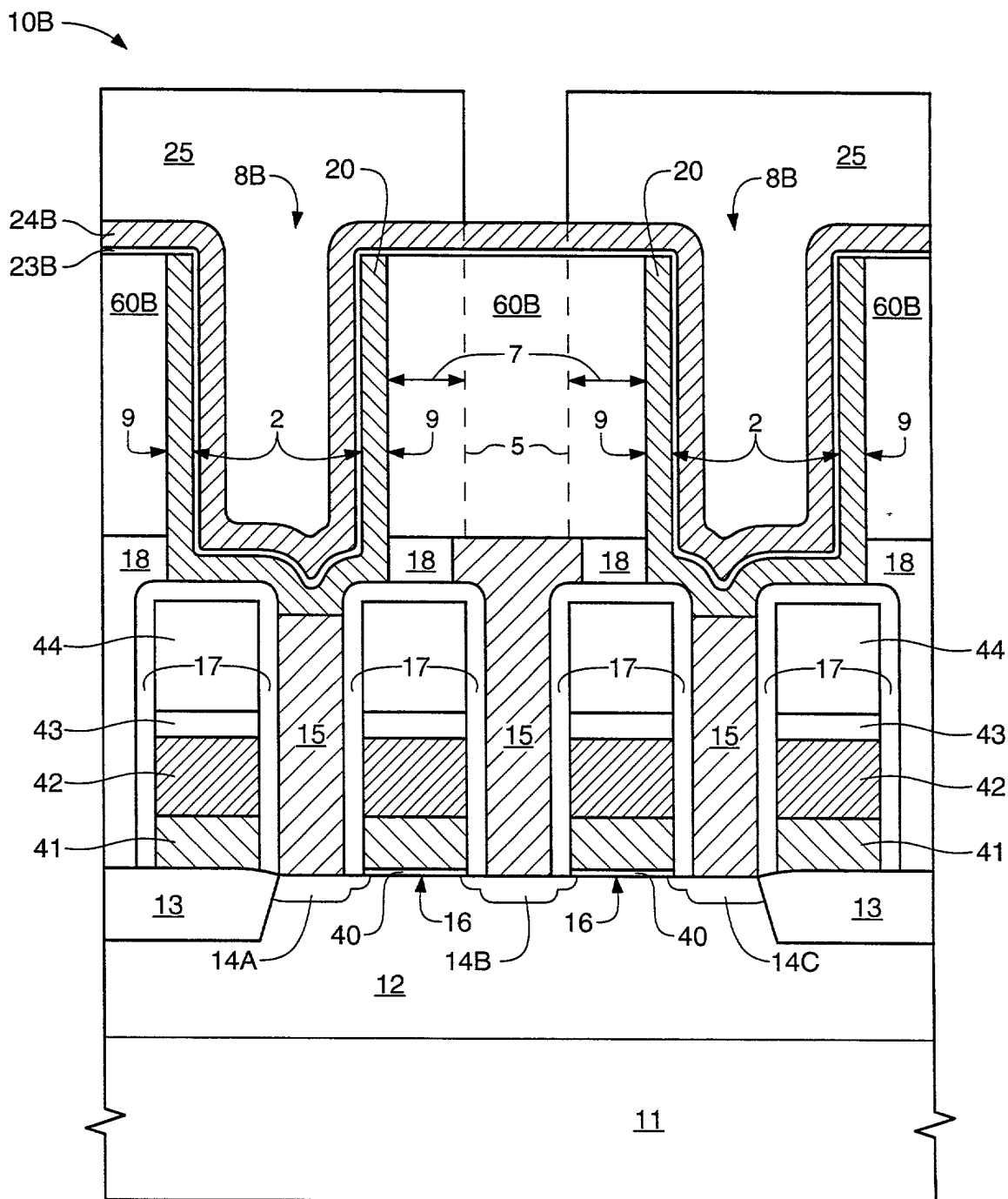


FIG. 3
(PRIOR ART)

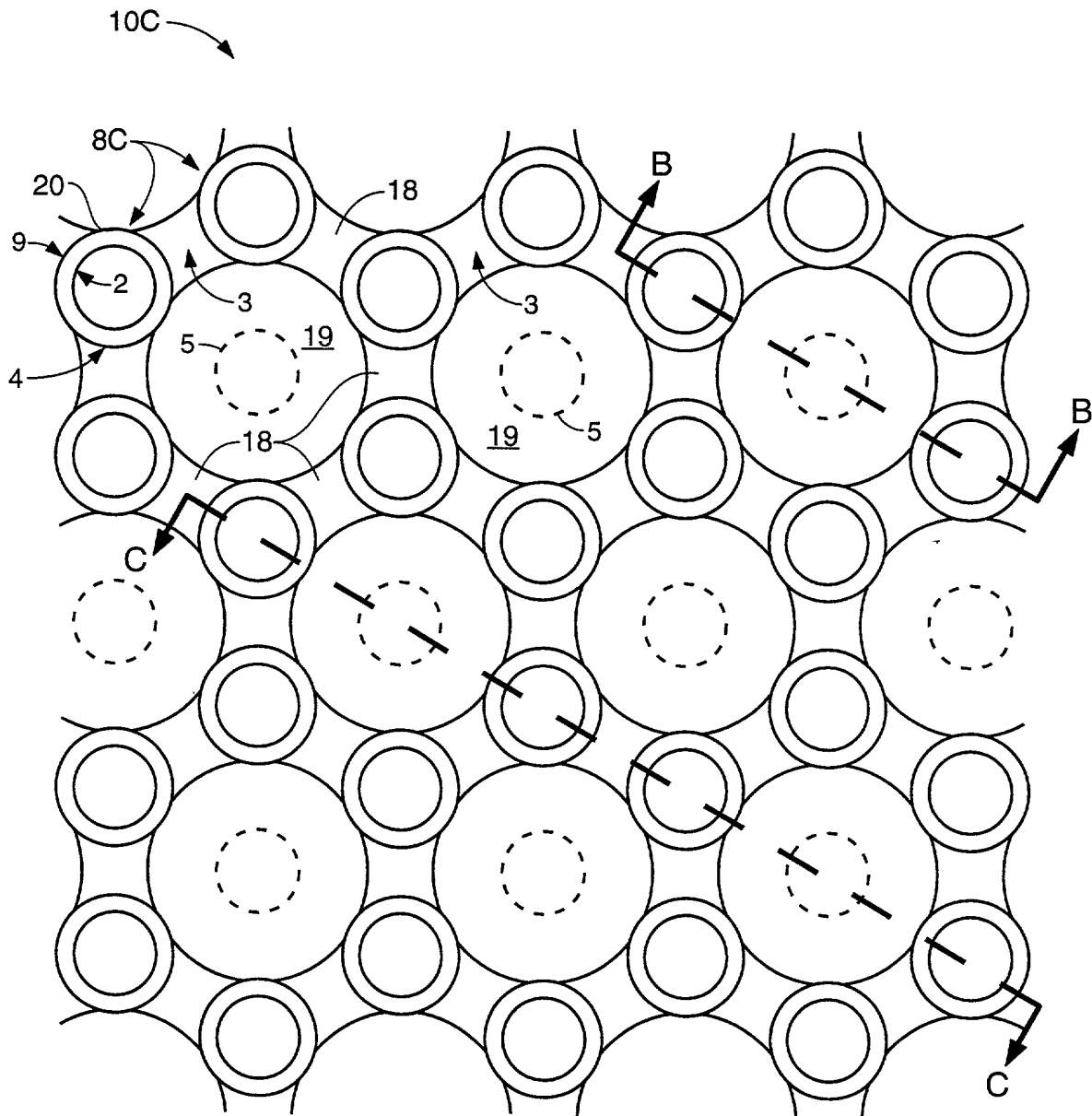


FIG. 4

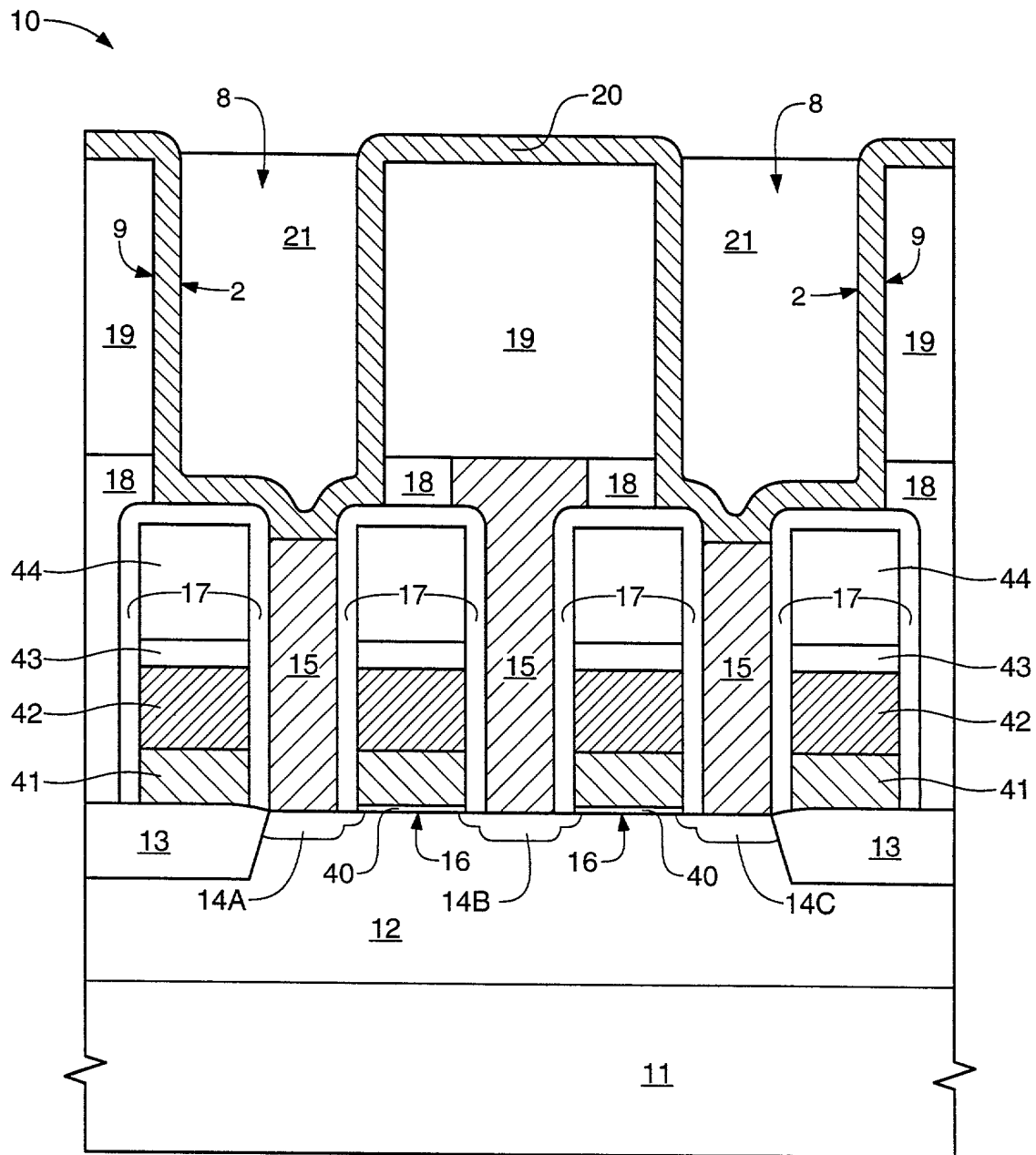


FIG. 5
(PRIOR ART)

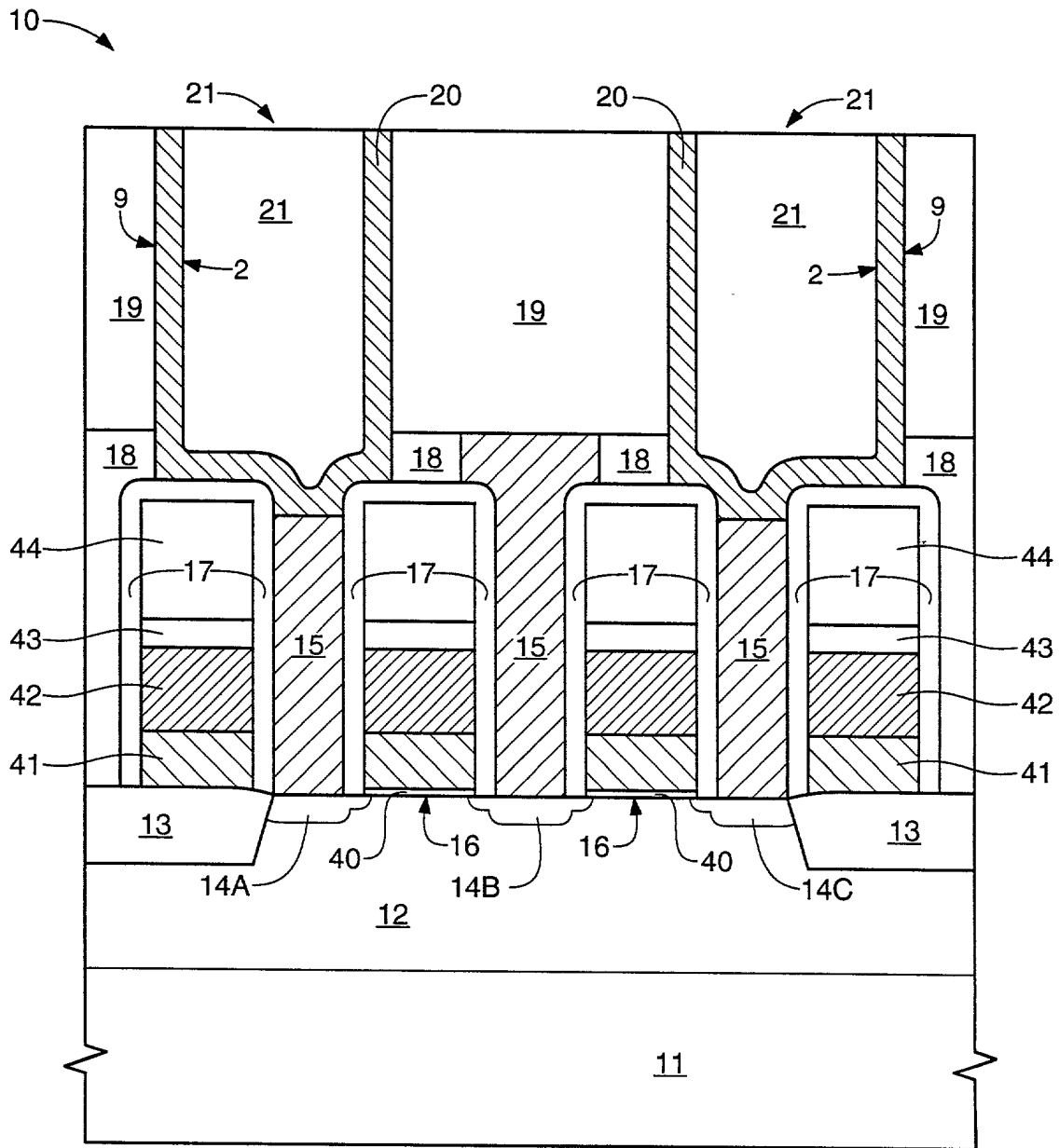
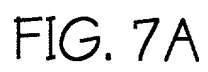


FIG. 6
(PRIOR ART)



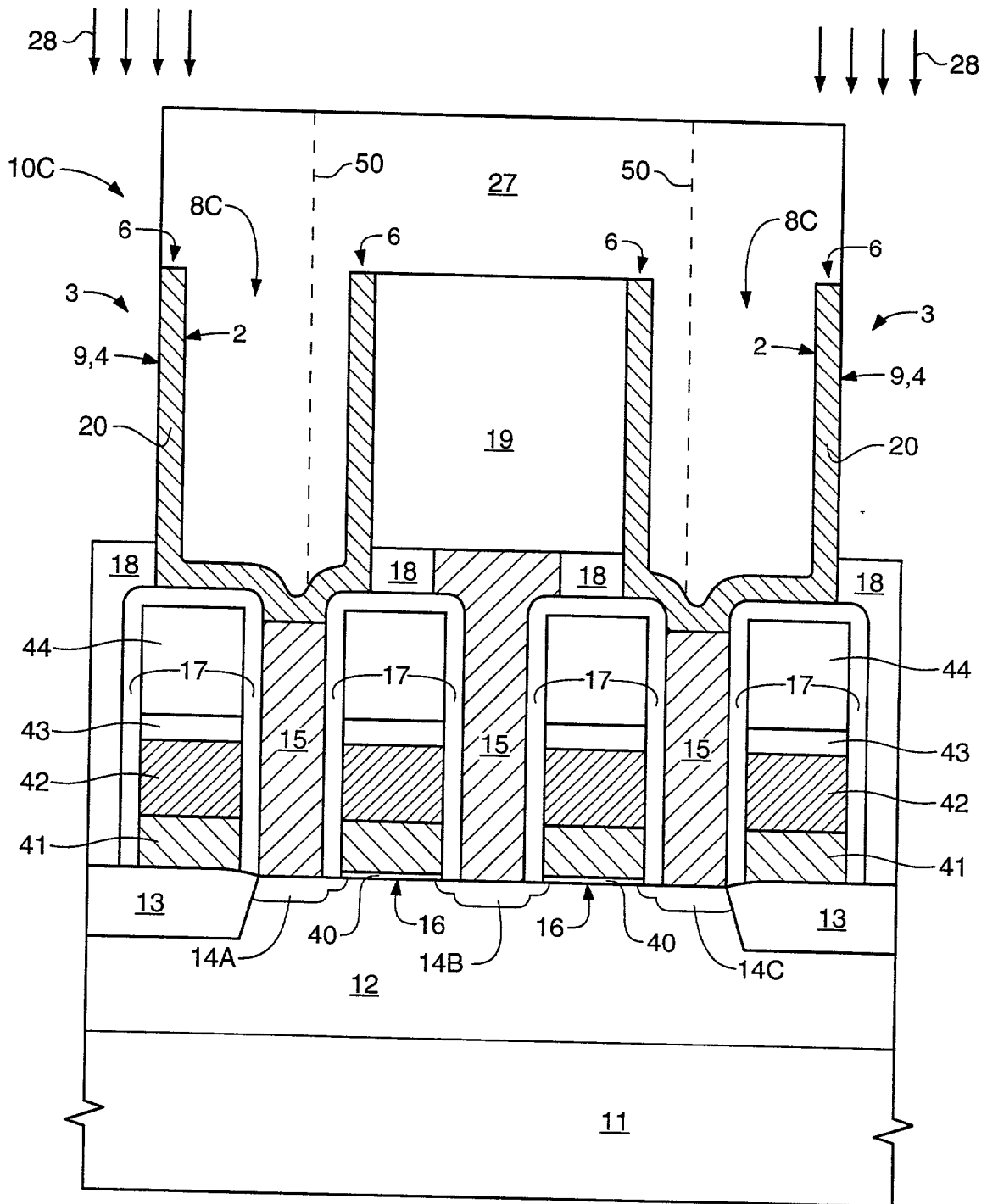


FIG. 7B

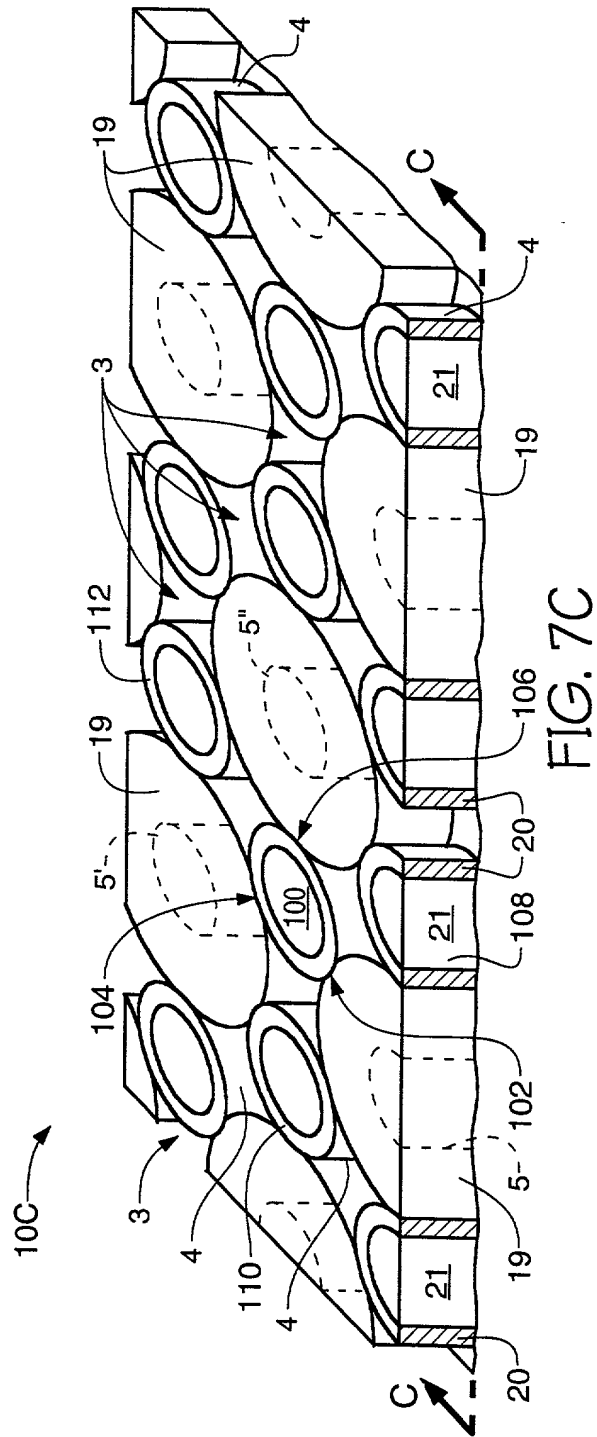


FIG. 7C

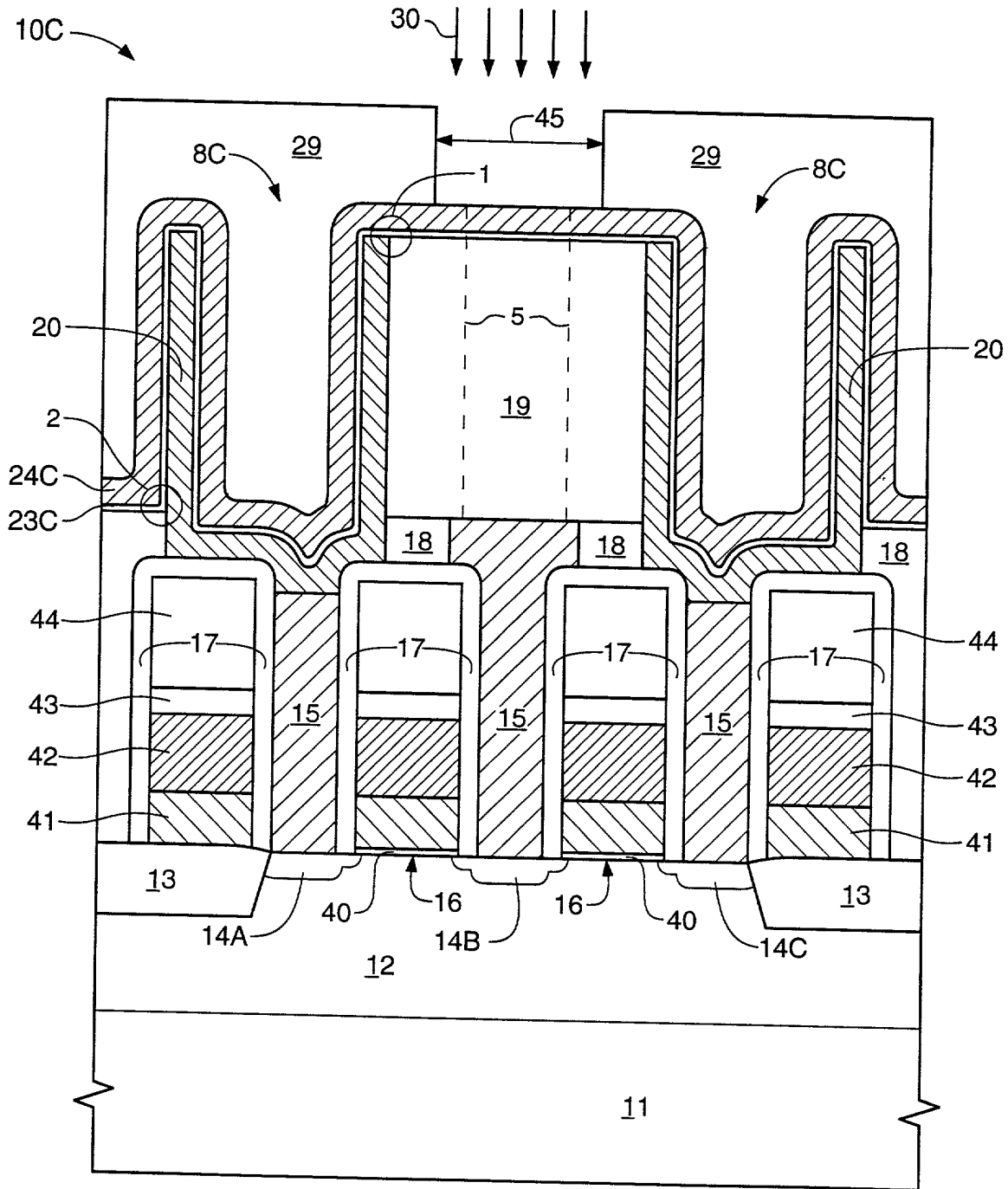


FIG. 8A

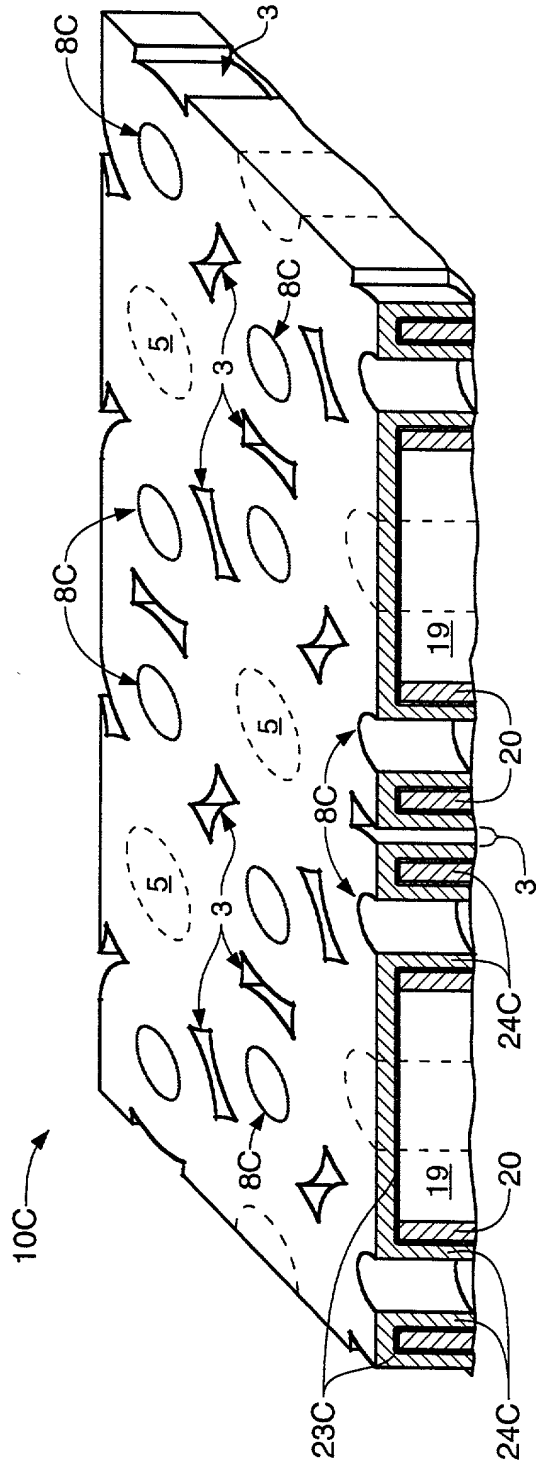


FIG. 8B



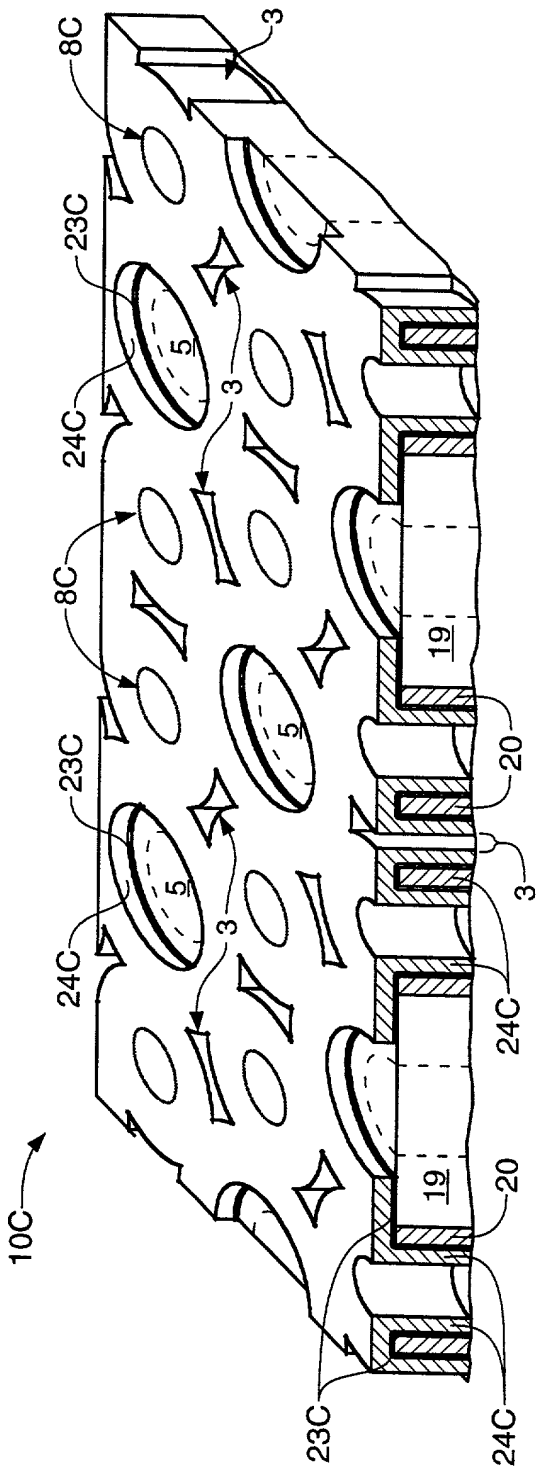
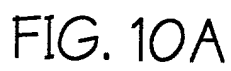
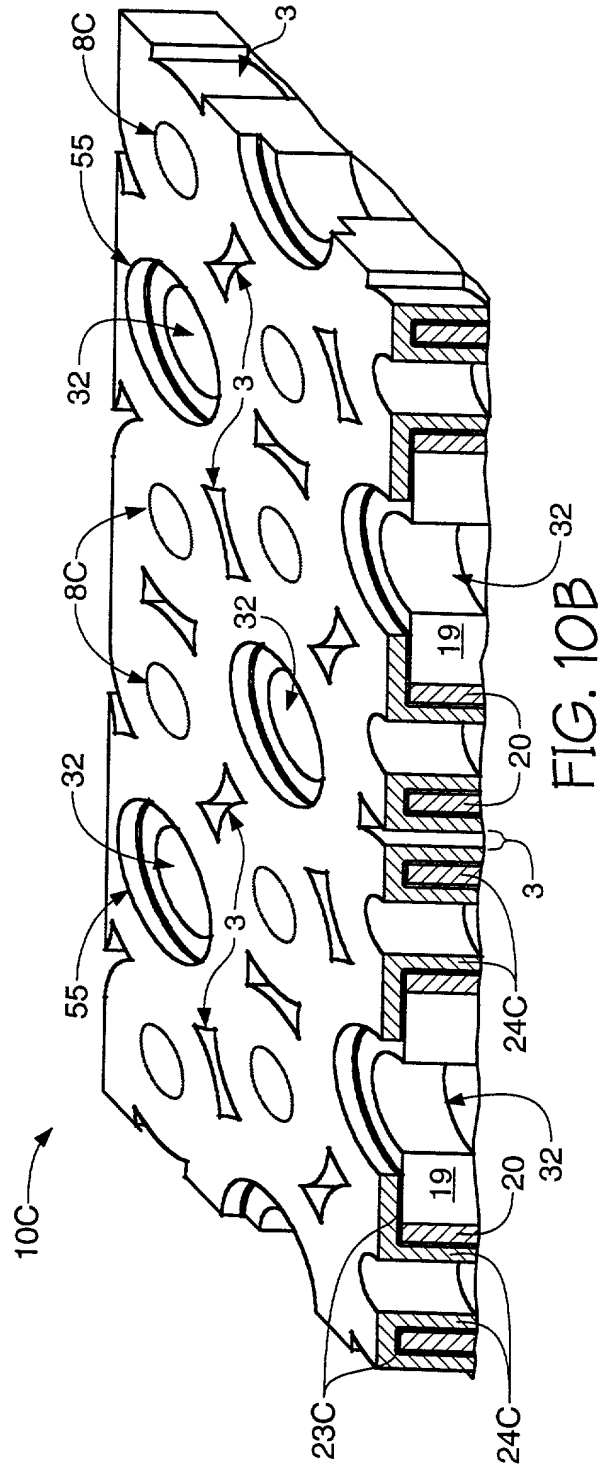


FIG. 9B





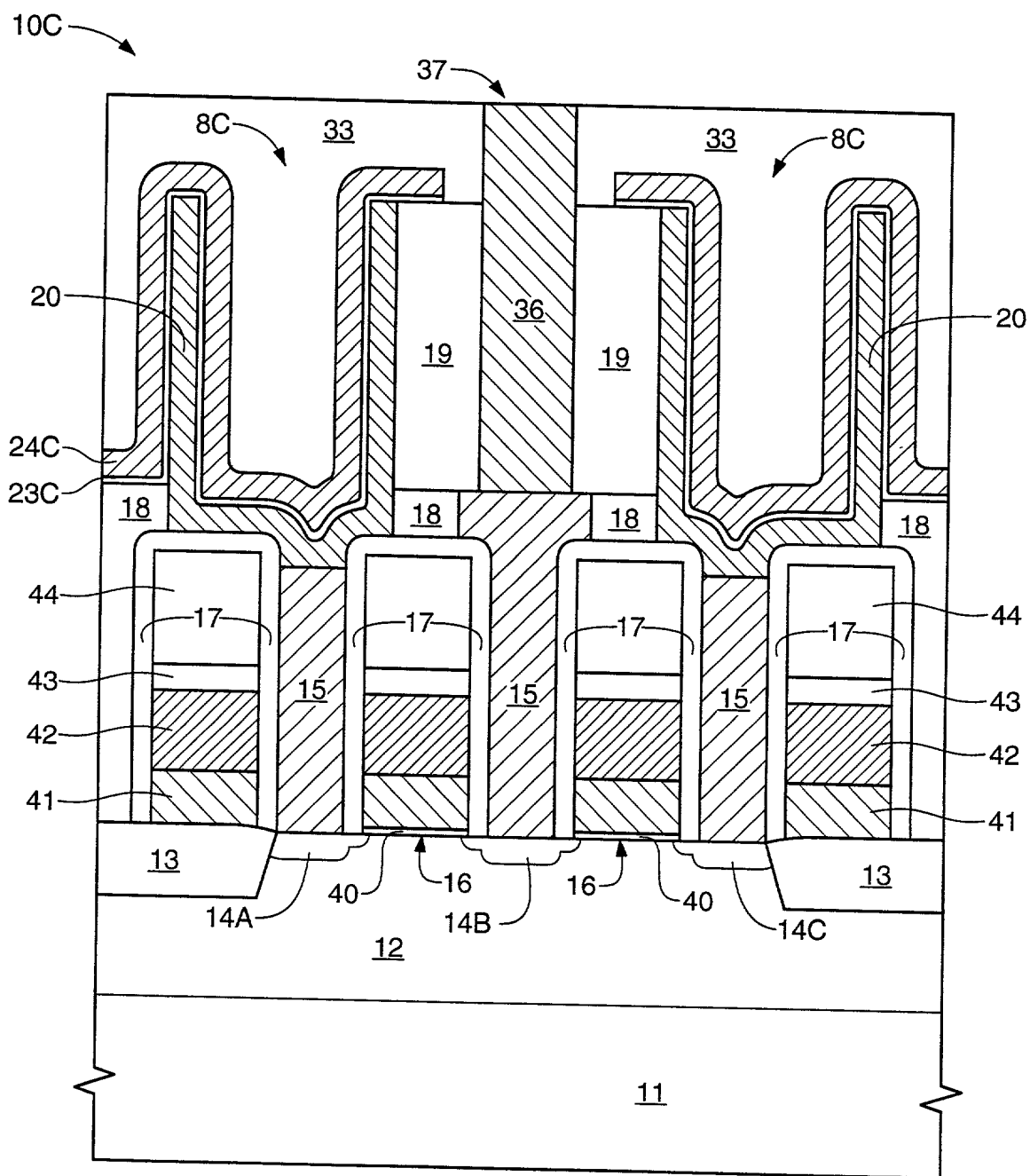
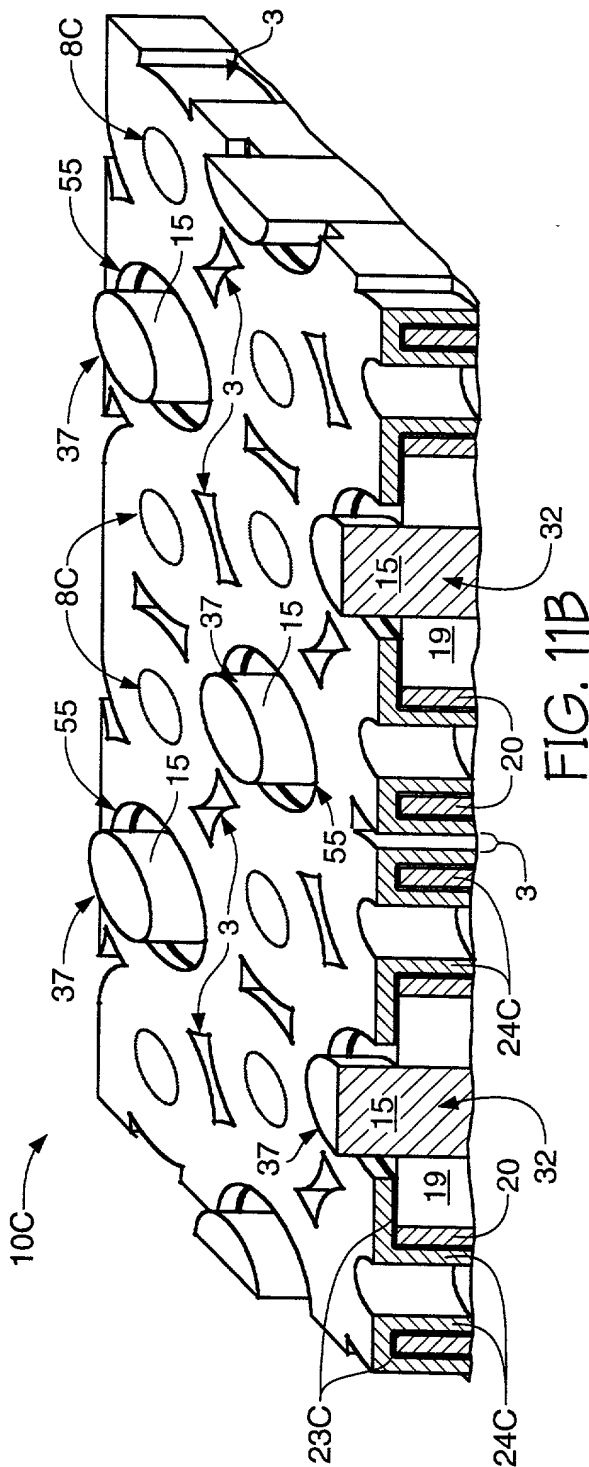


FIG. 11A



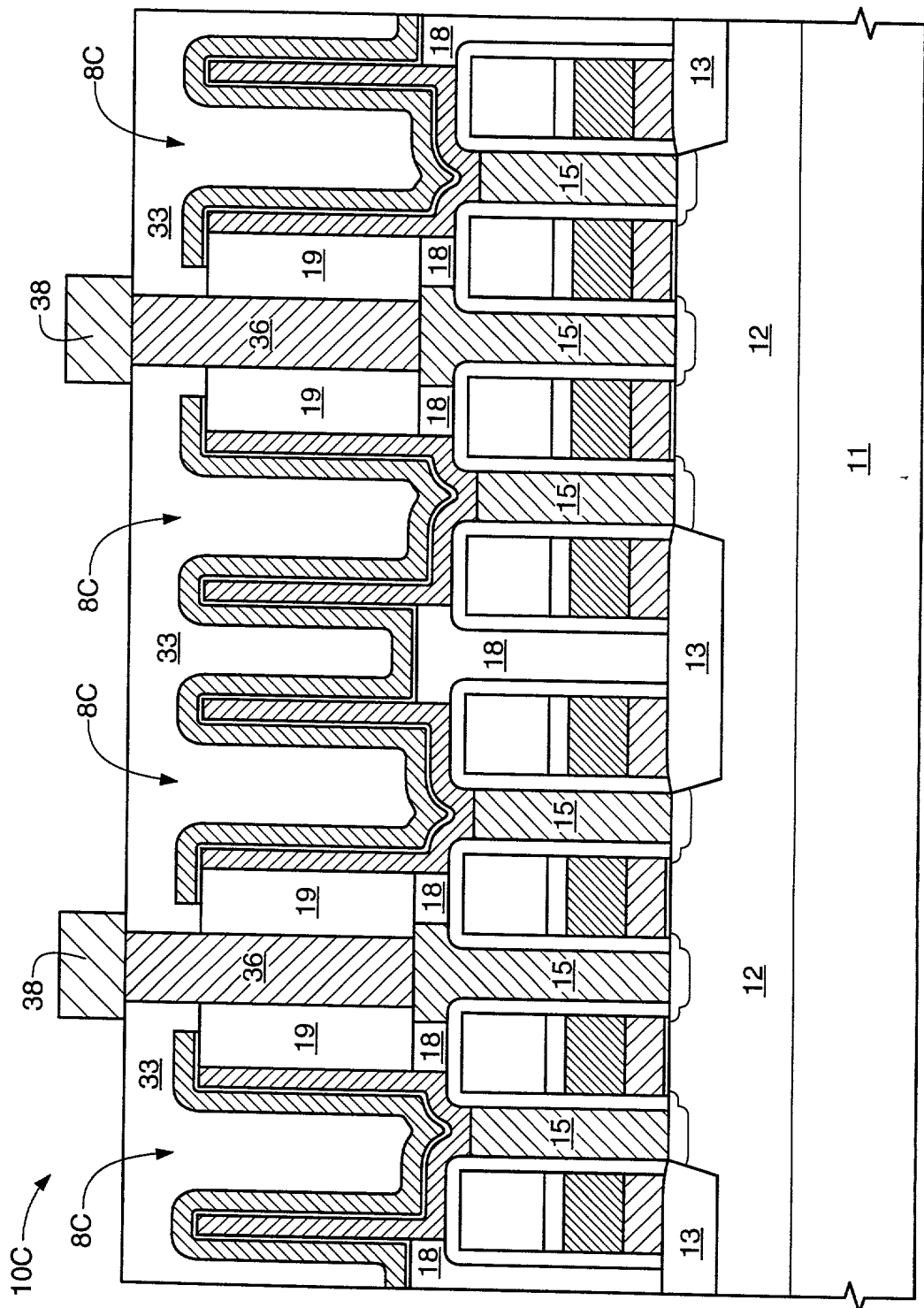


FIG. 12

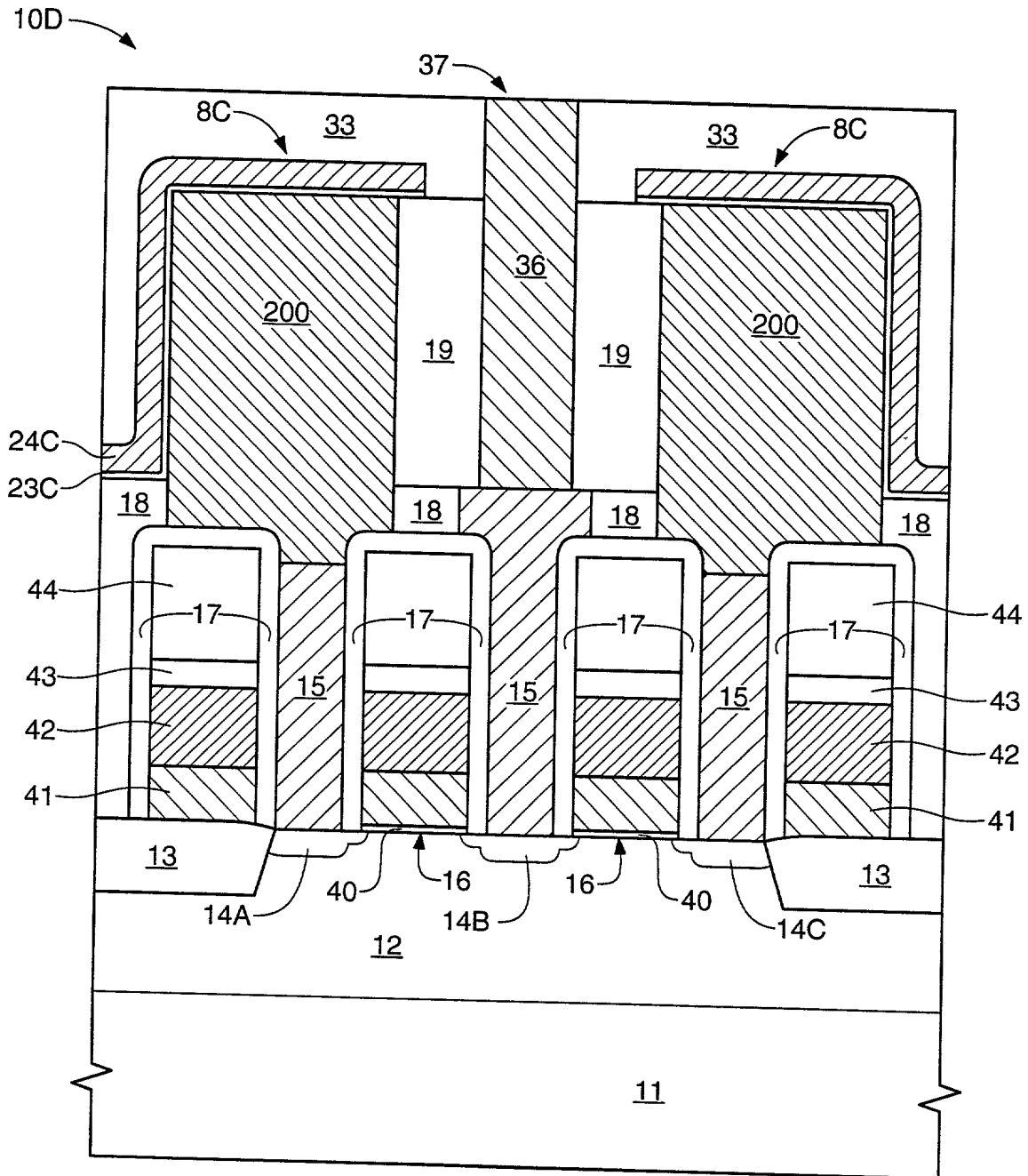


FIG. 13

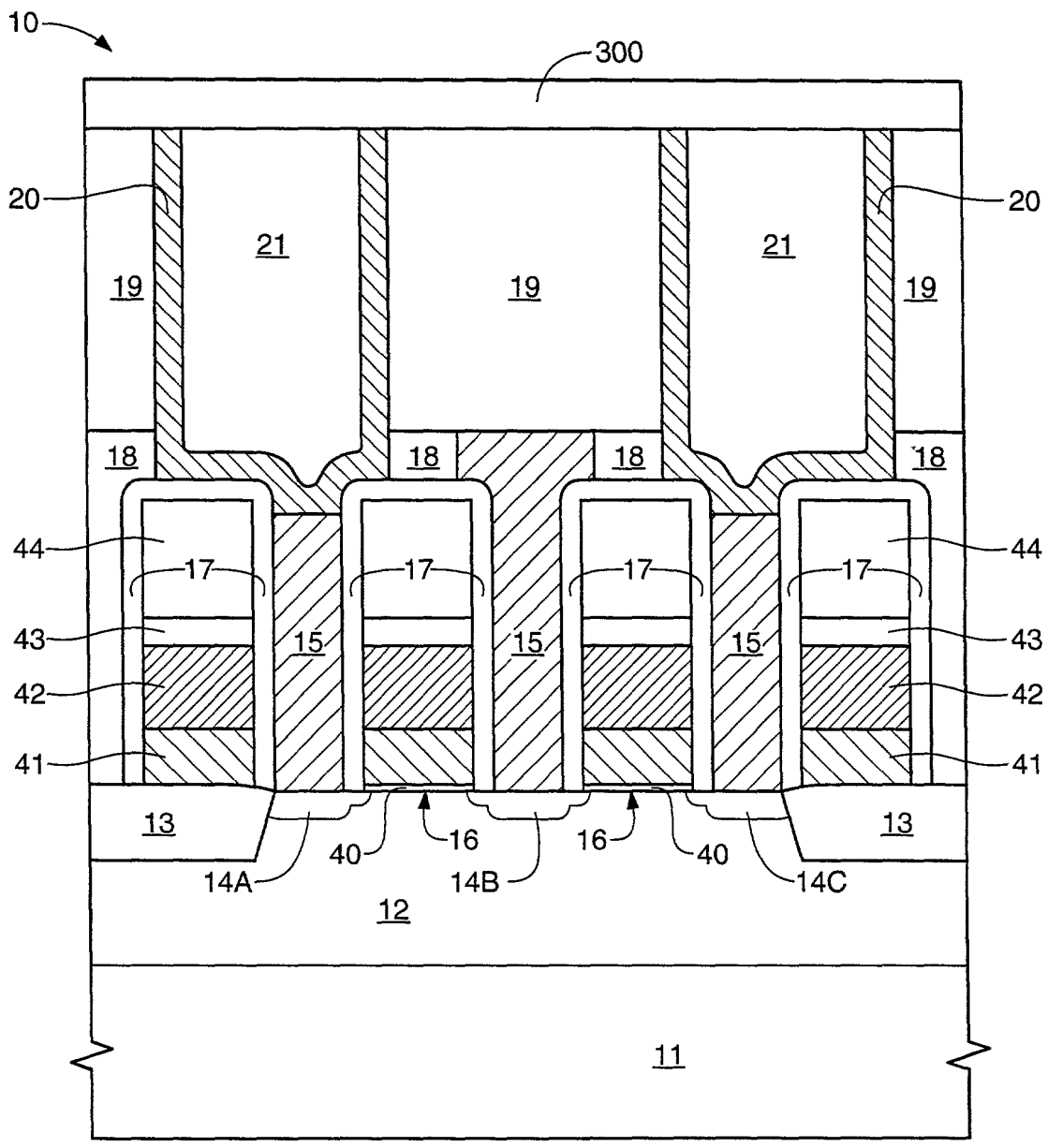


FIG. 14A

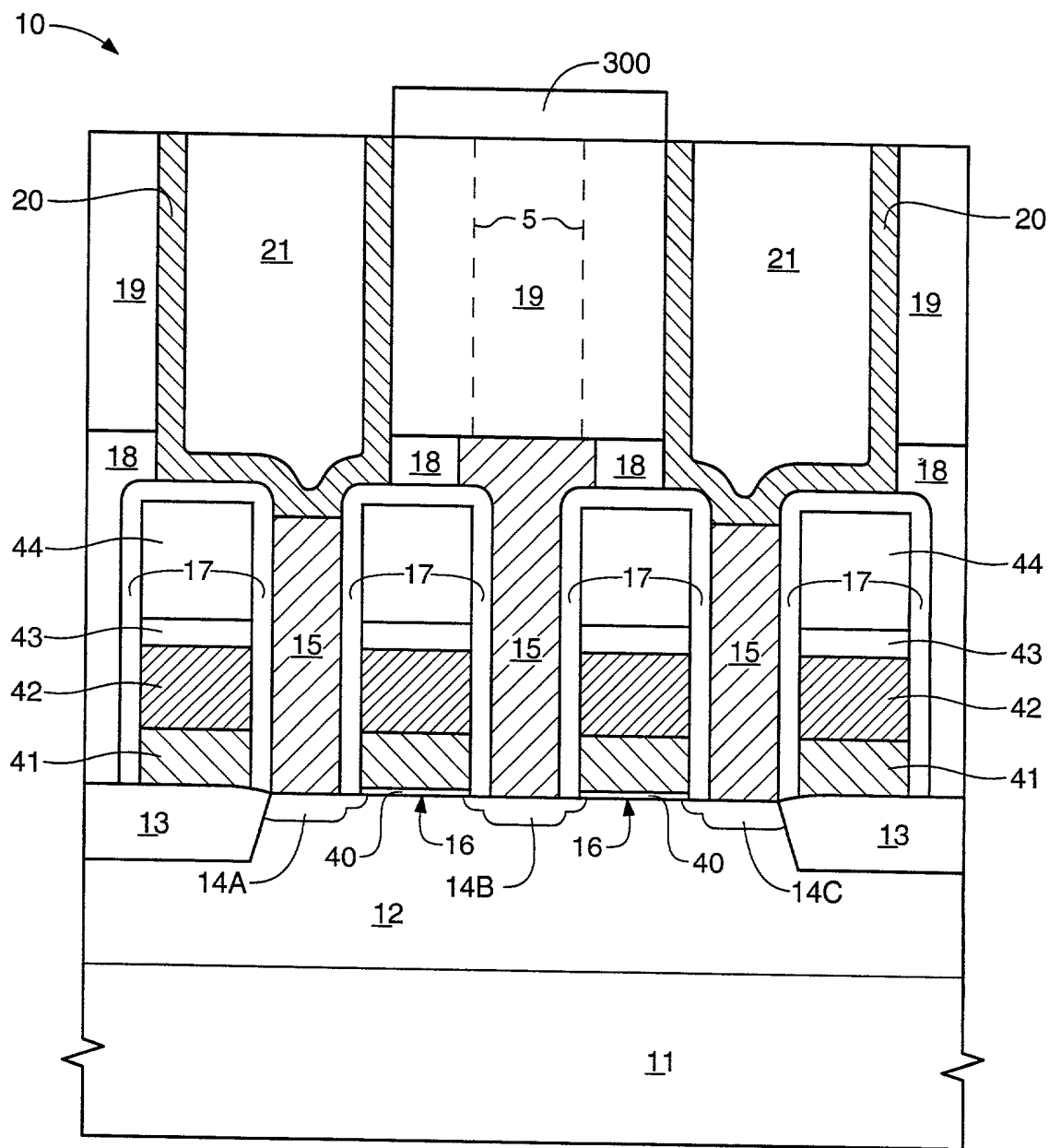


FIG. 14B

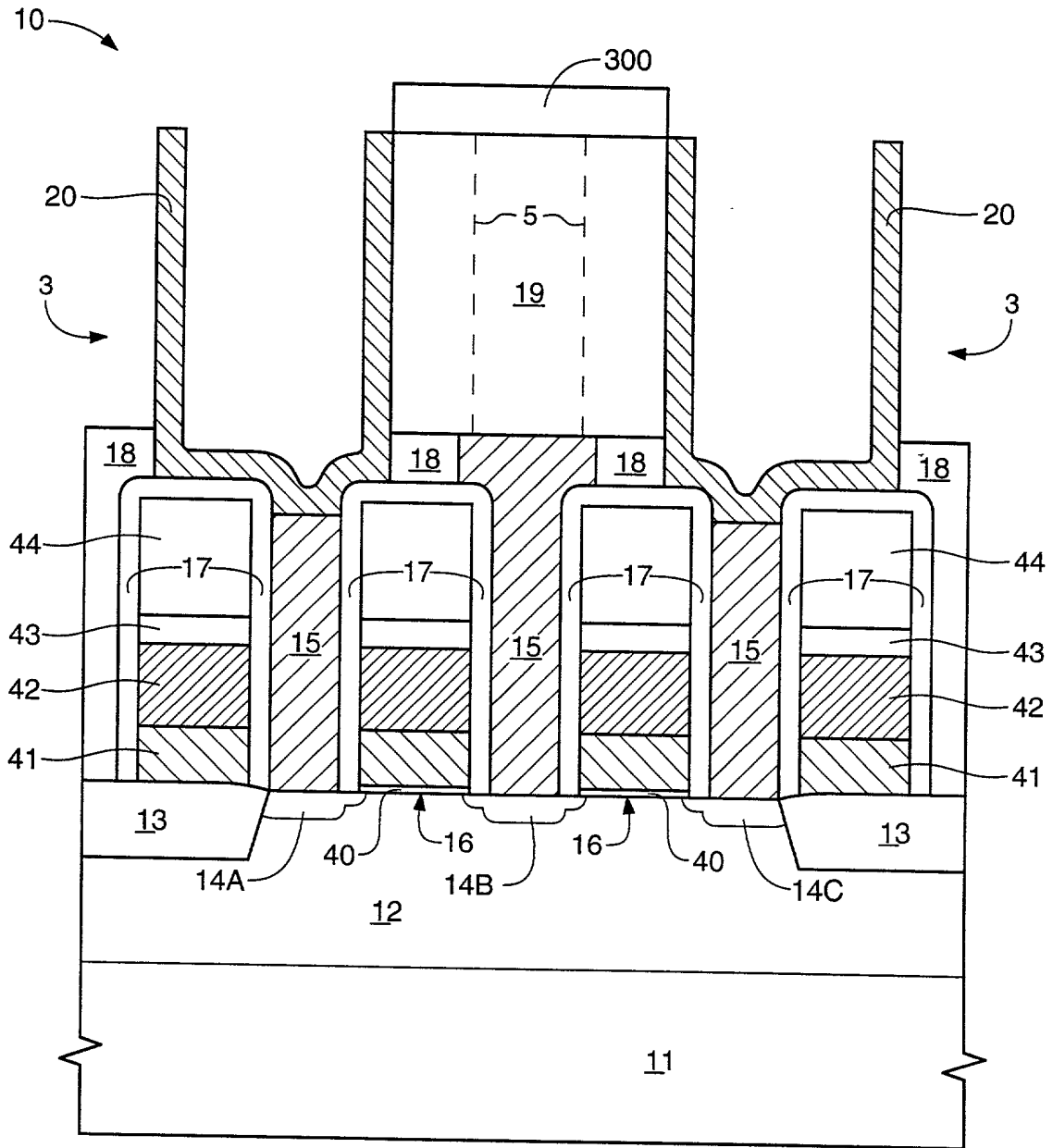


FIG. 14C

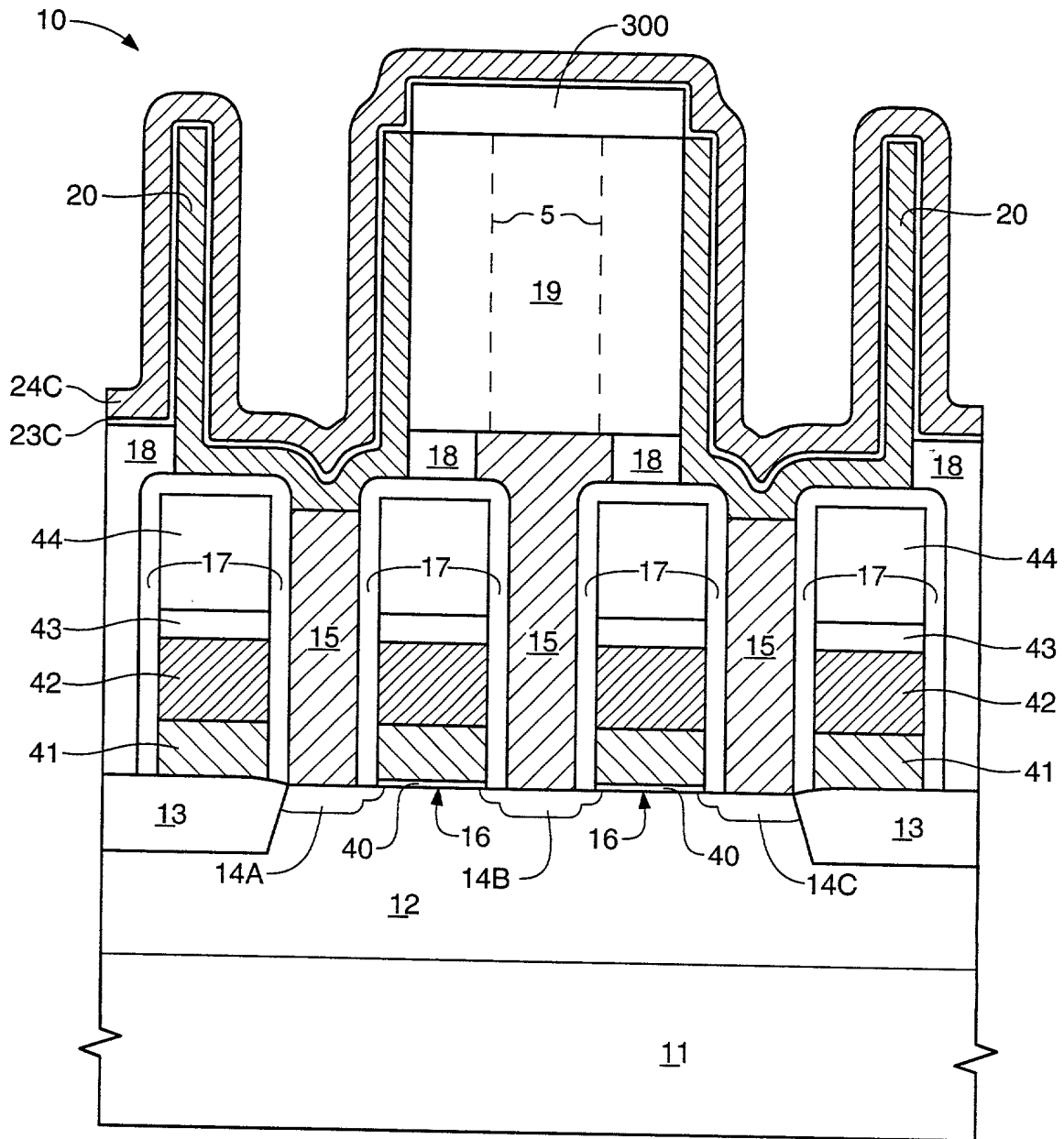


FIG. 14D

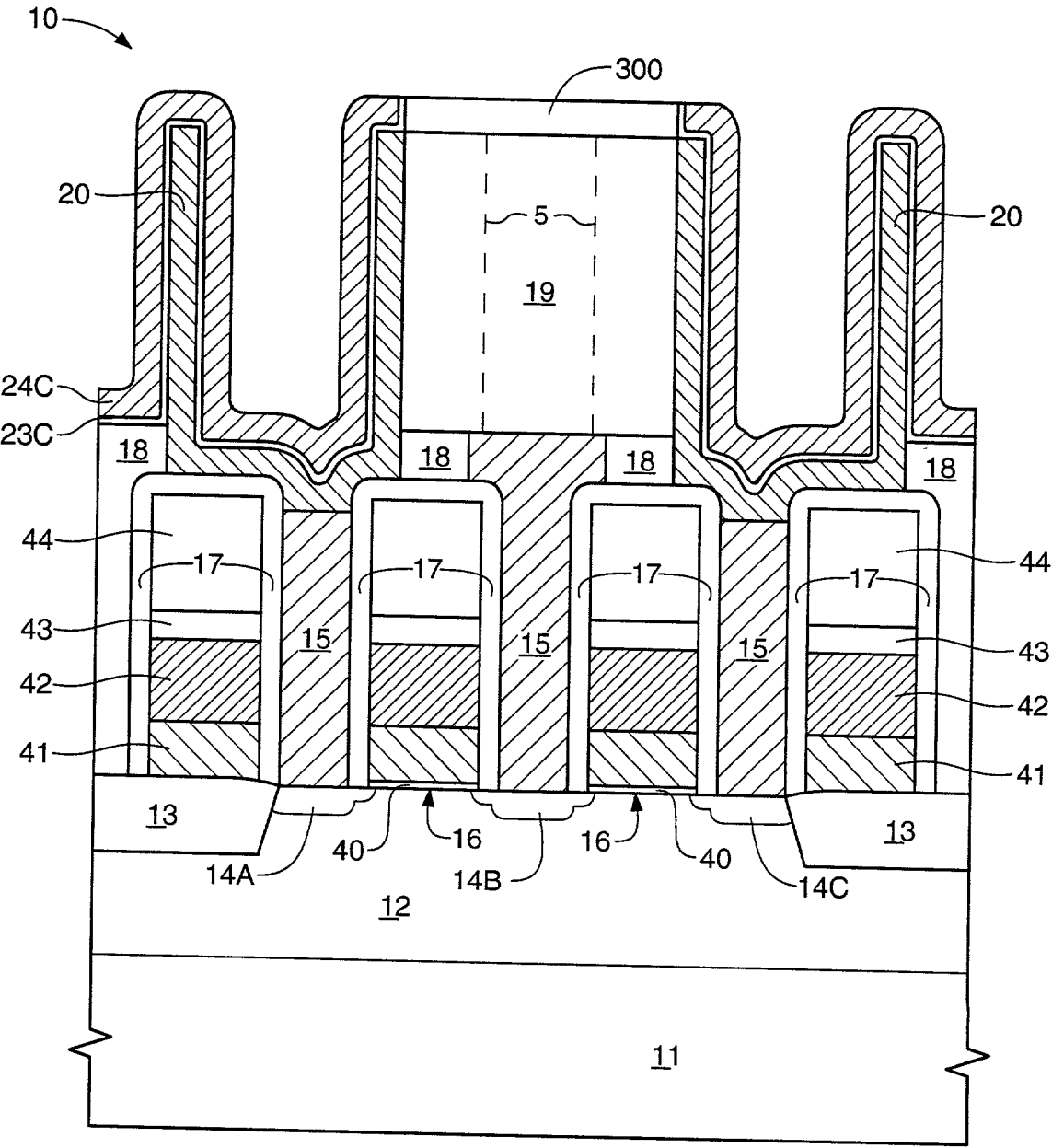


FIG. 14E

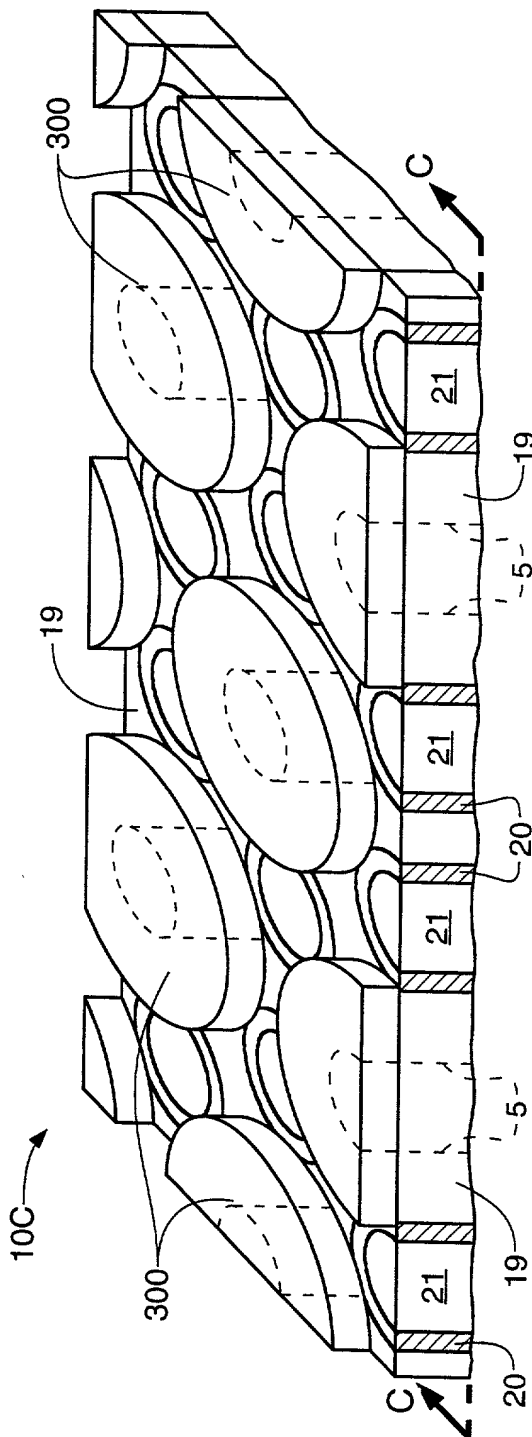


FIG. 14F

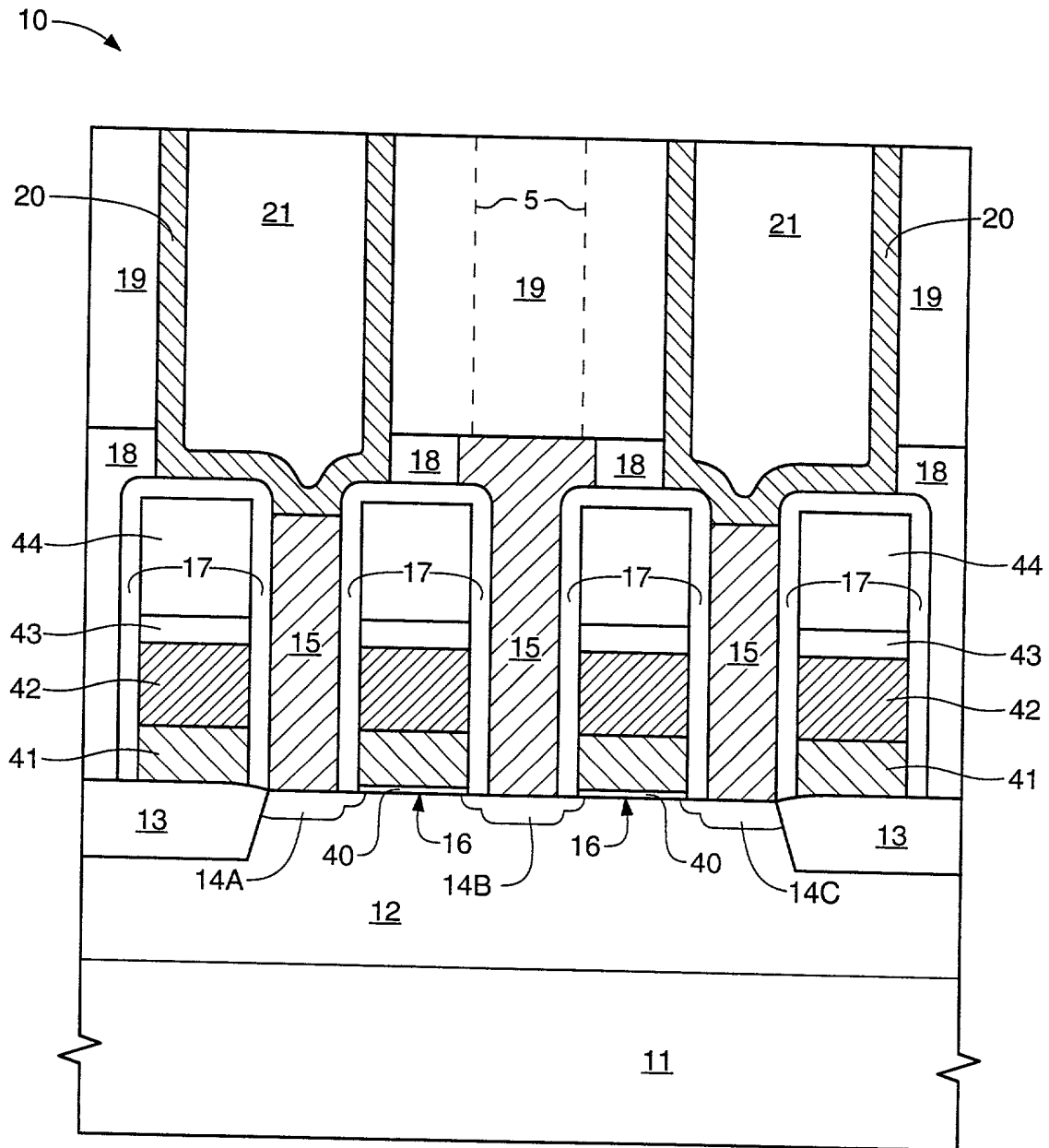


FIG. 15A

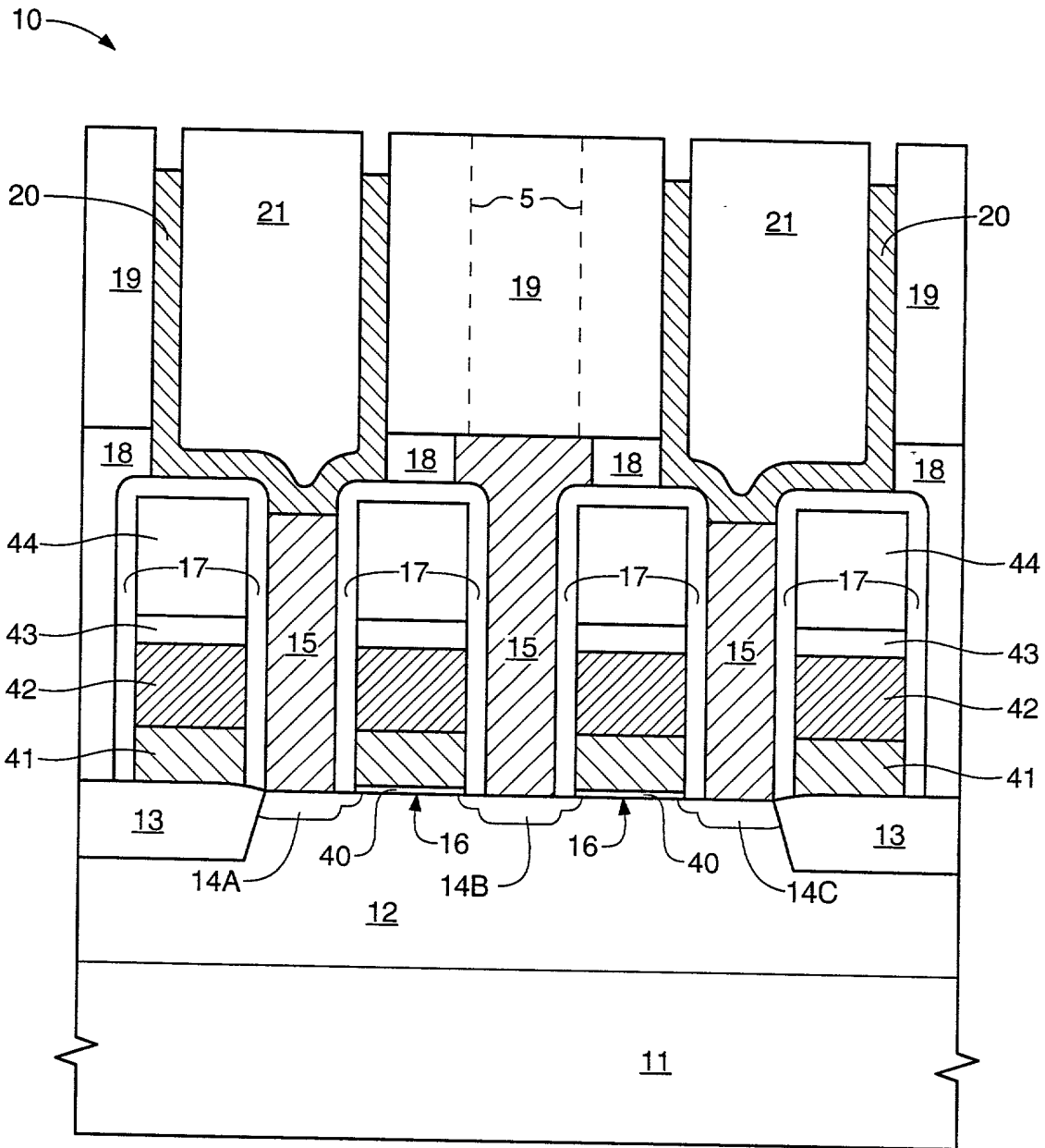


FIG. 15B

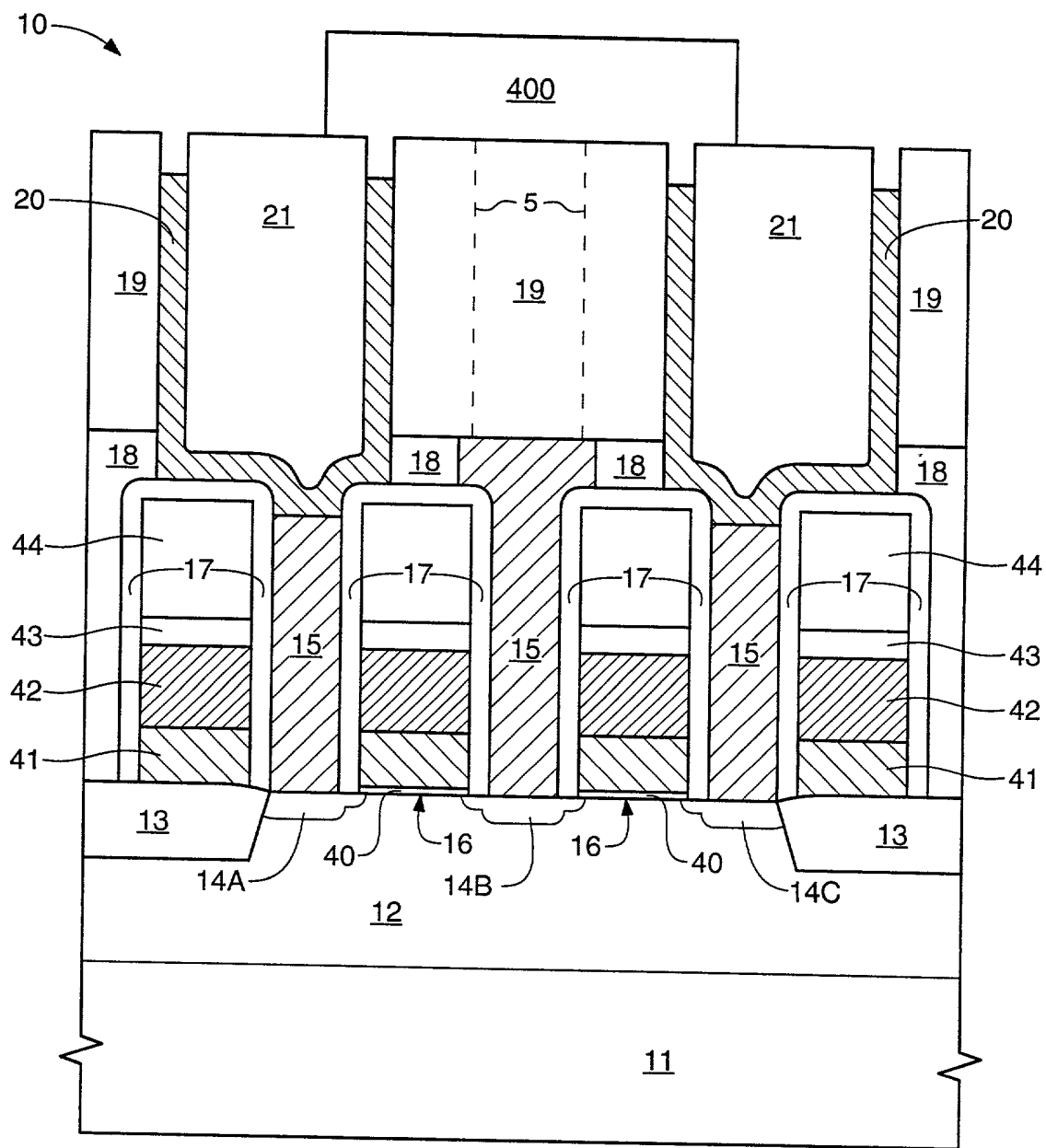


FIG. 15C

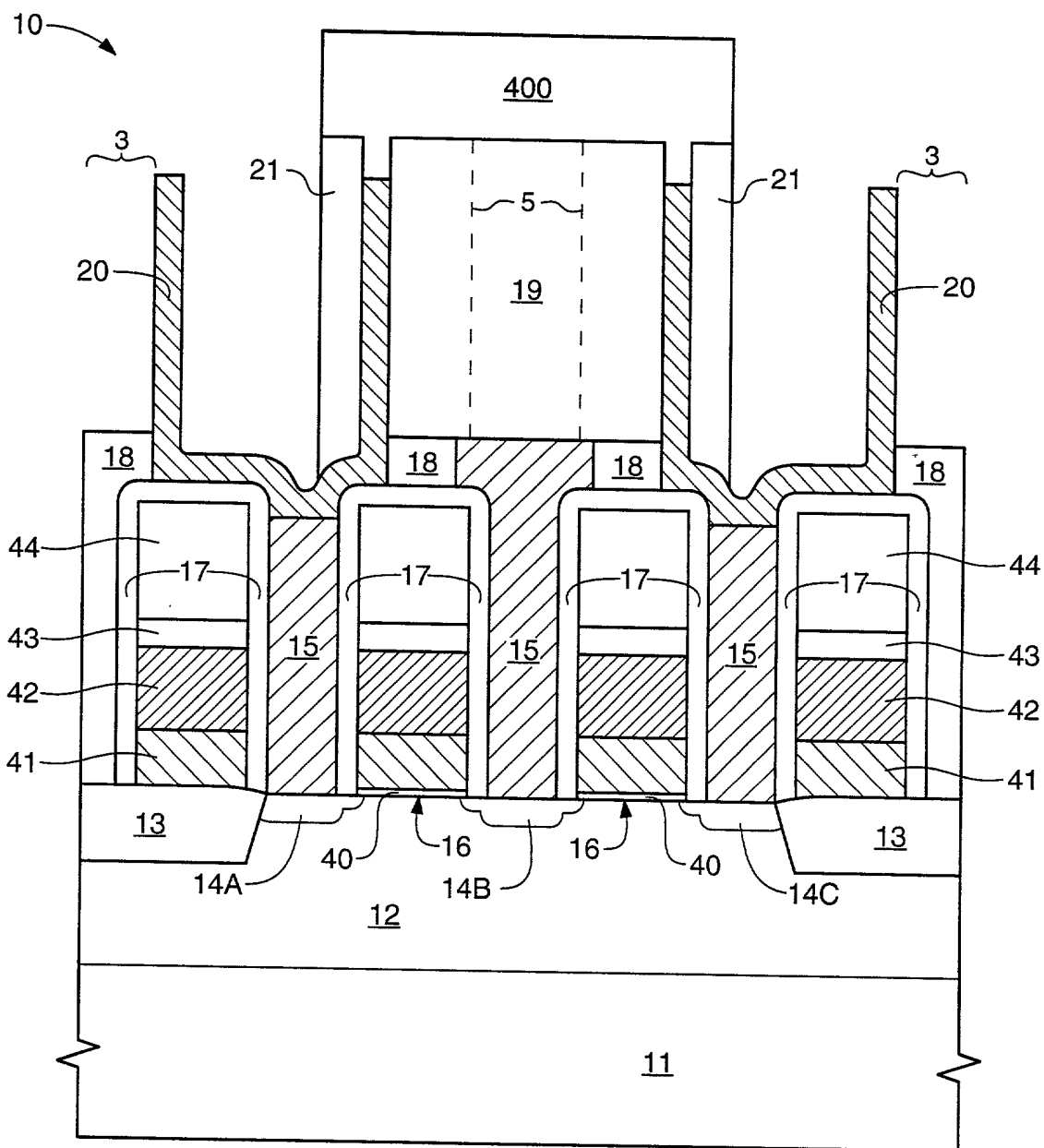


FIG. 15D

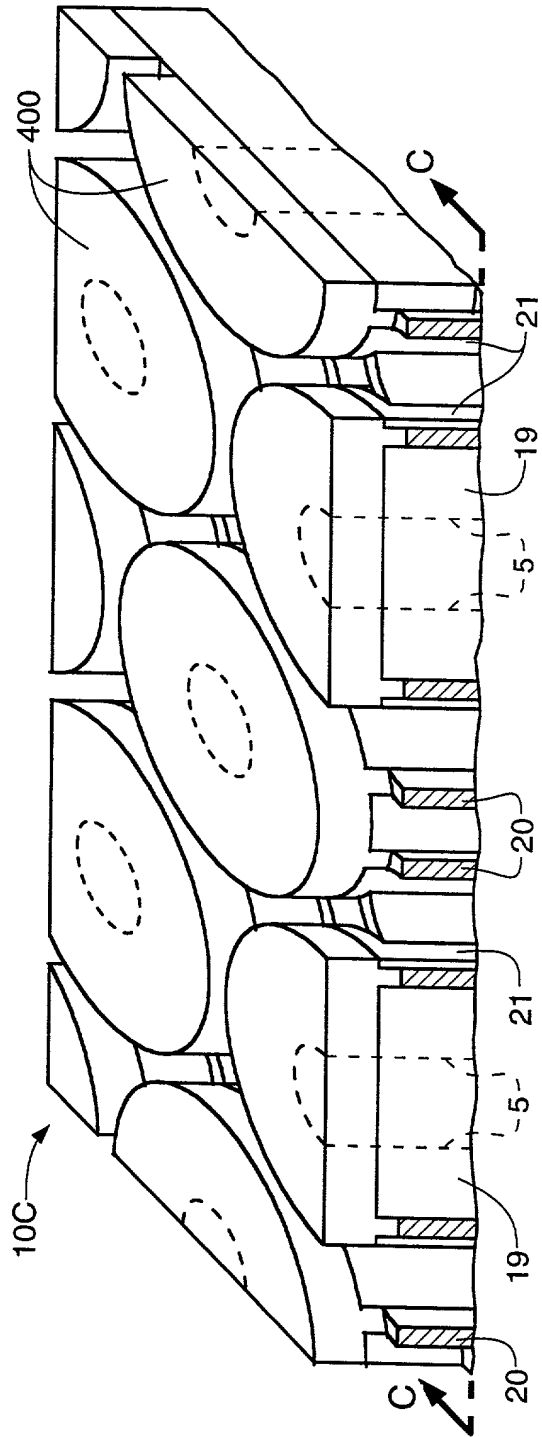


FIG. 15E

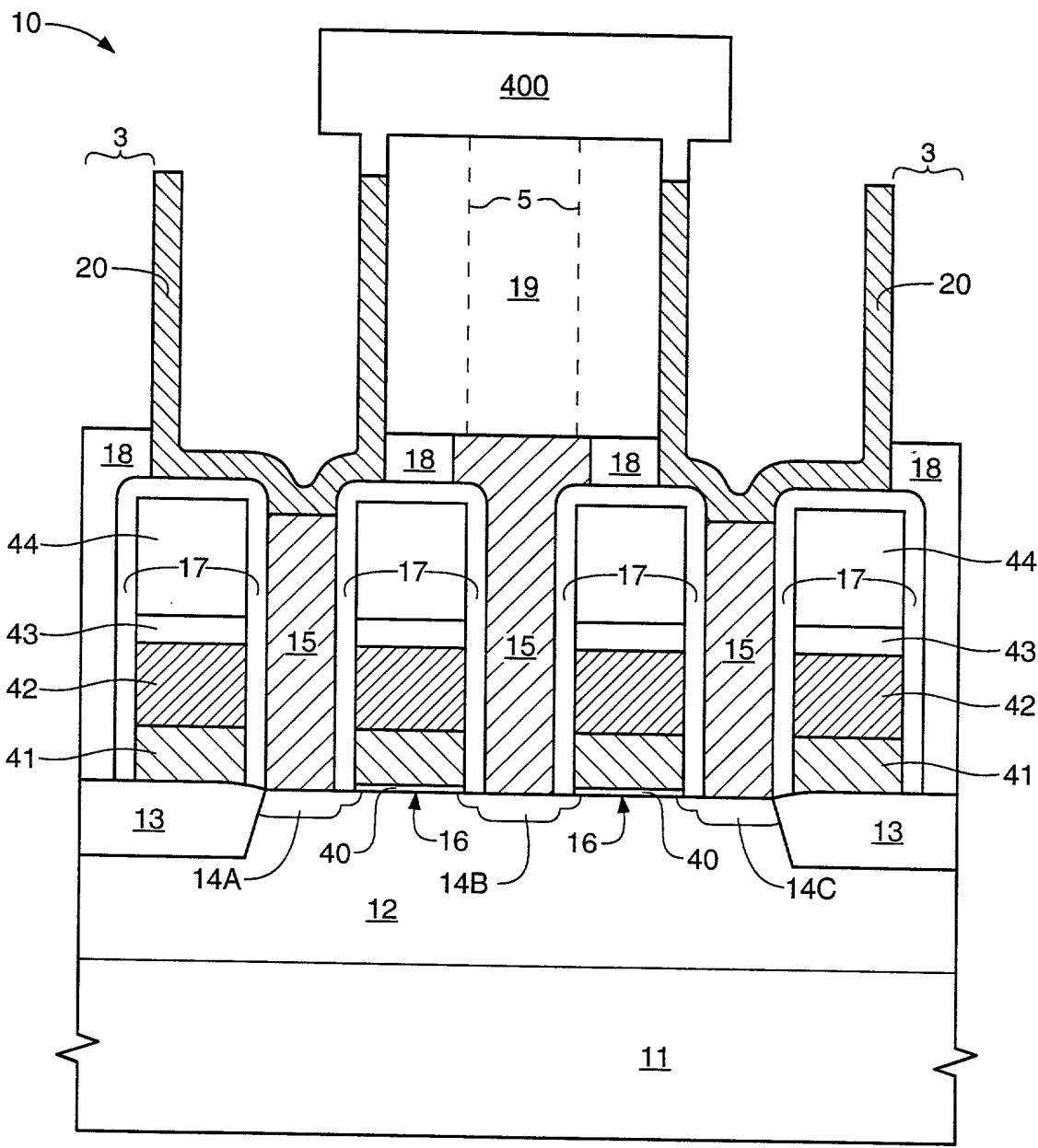
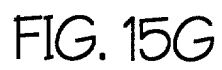


FIG. 15F



10

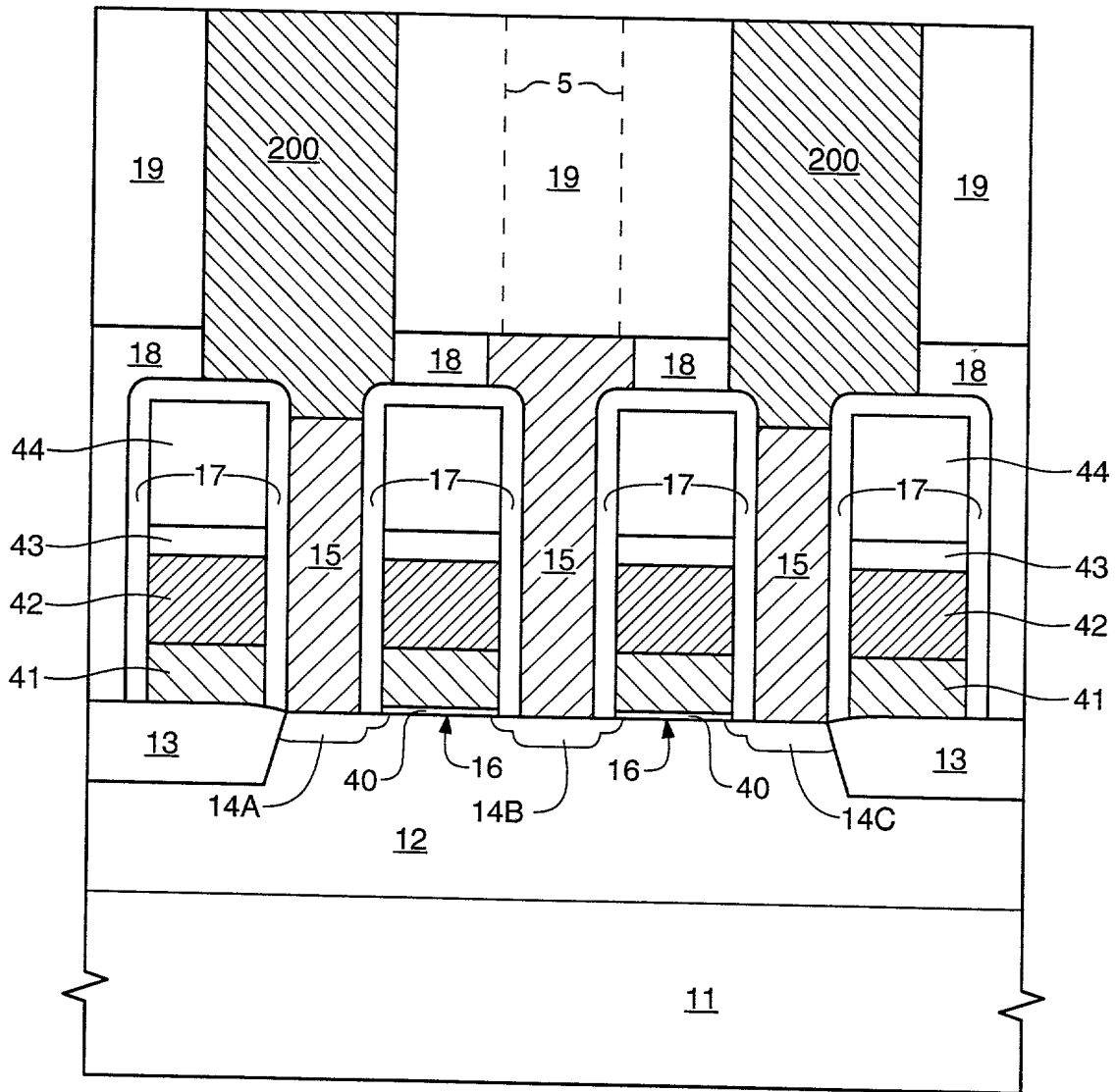
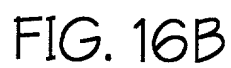


FIG. 16A



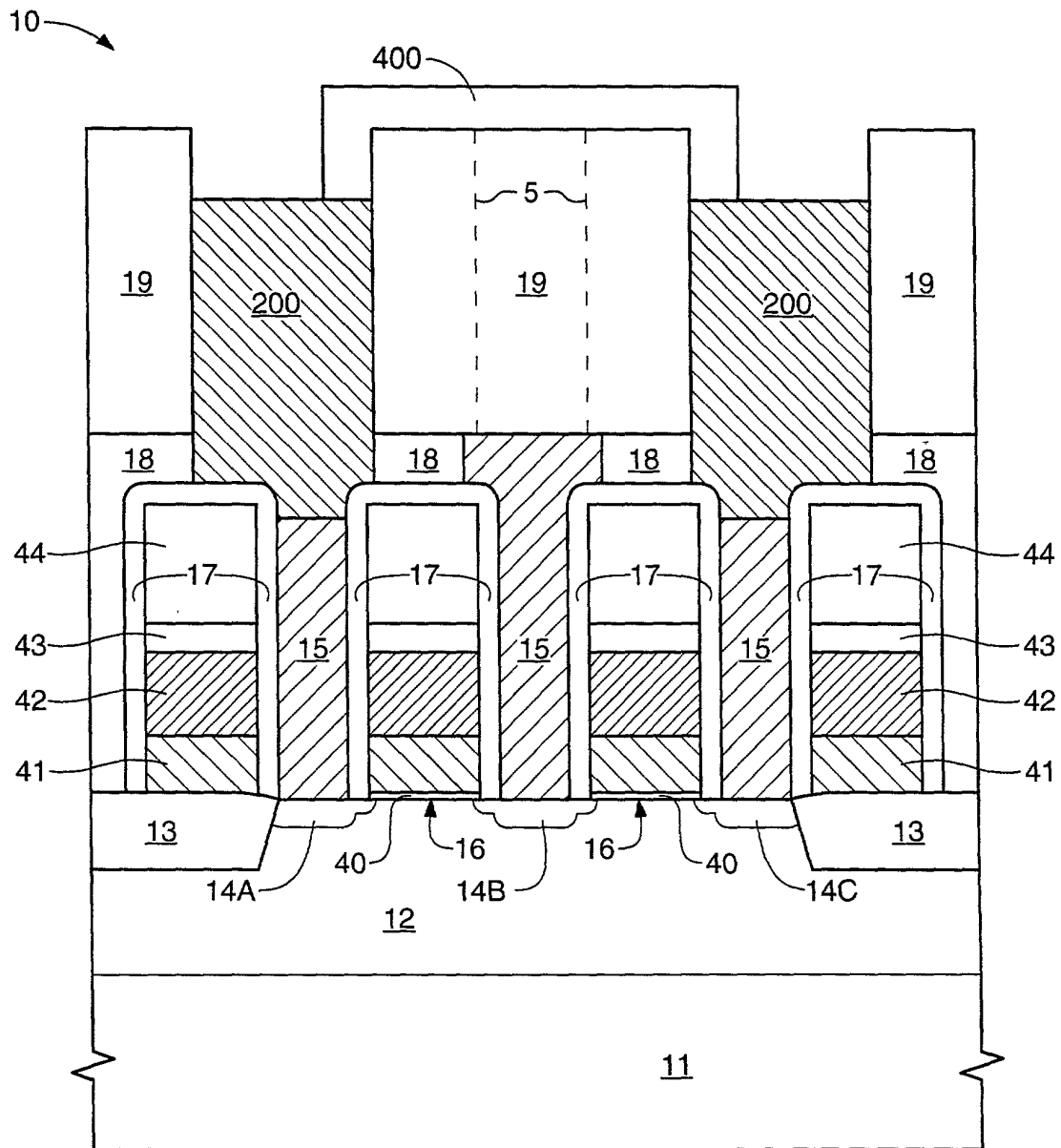


FIG. 16C

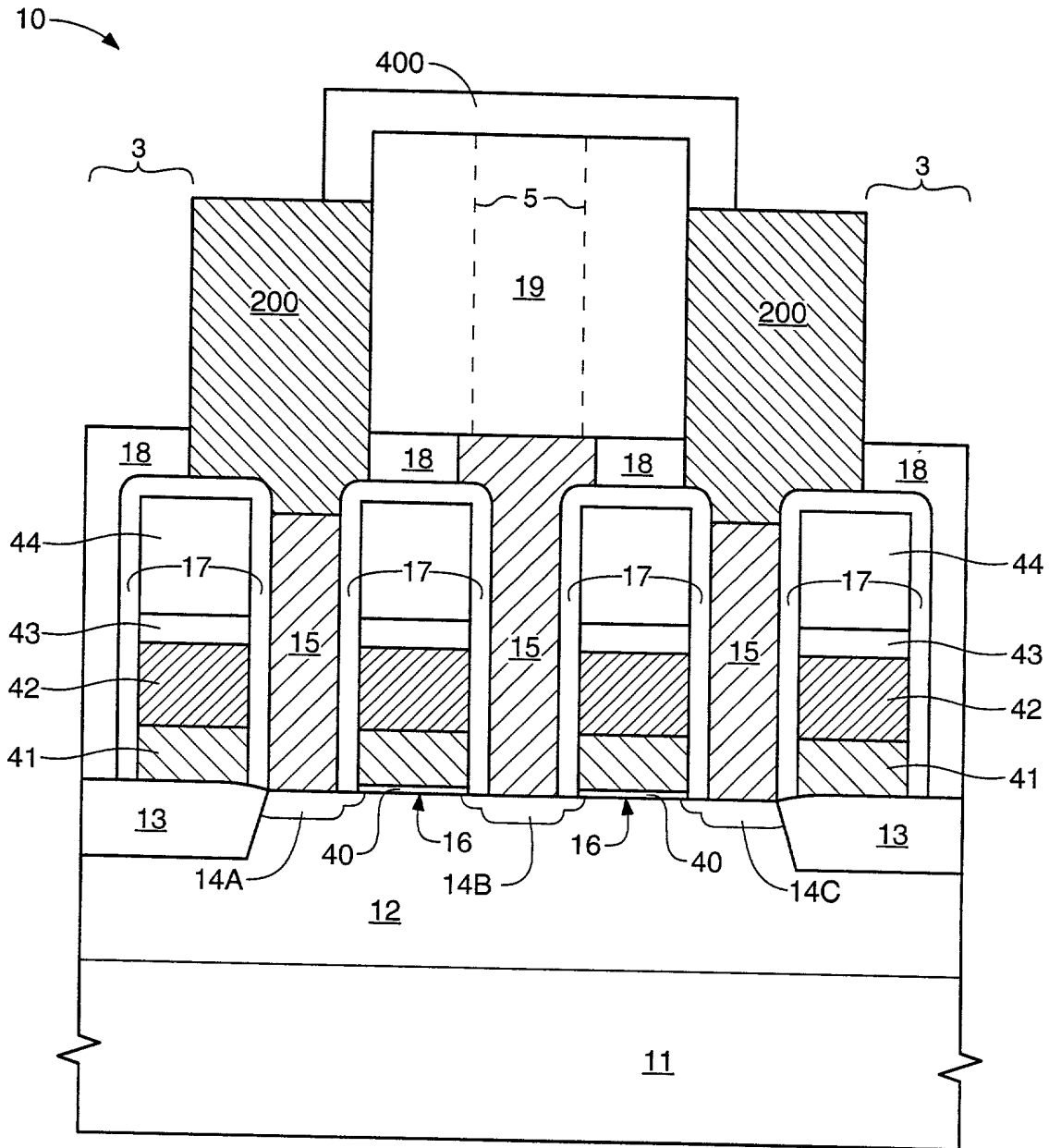
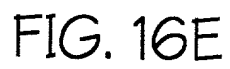


FIG. 16D



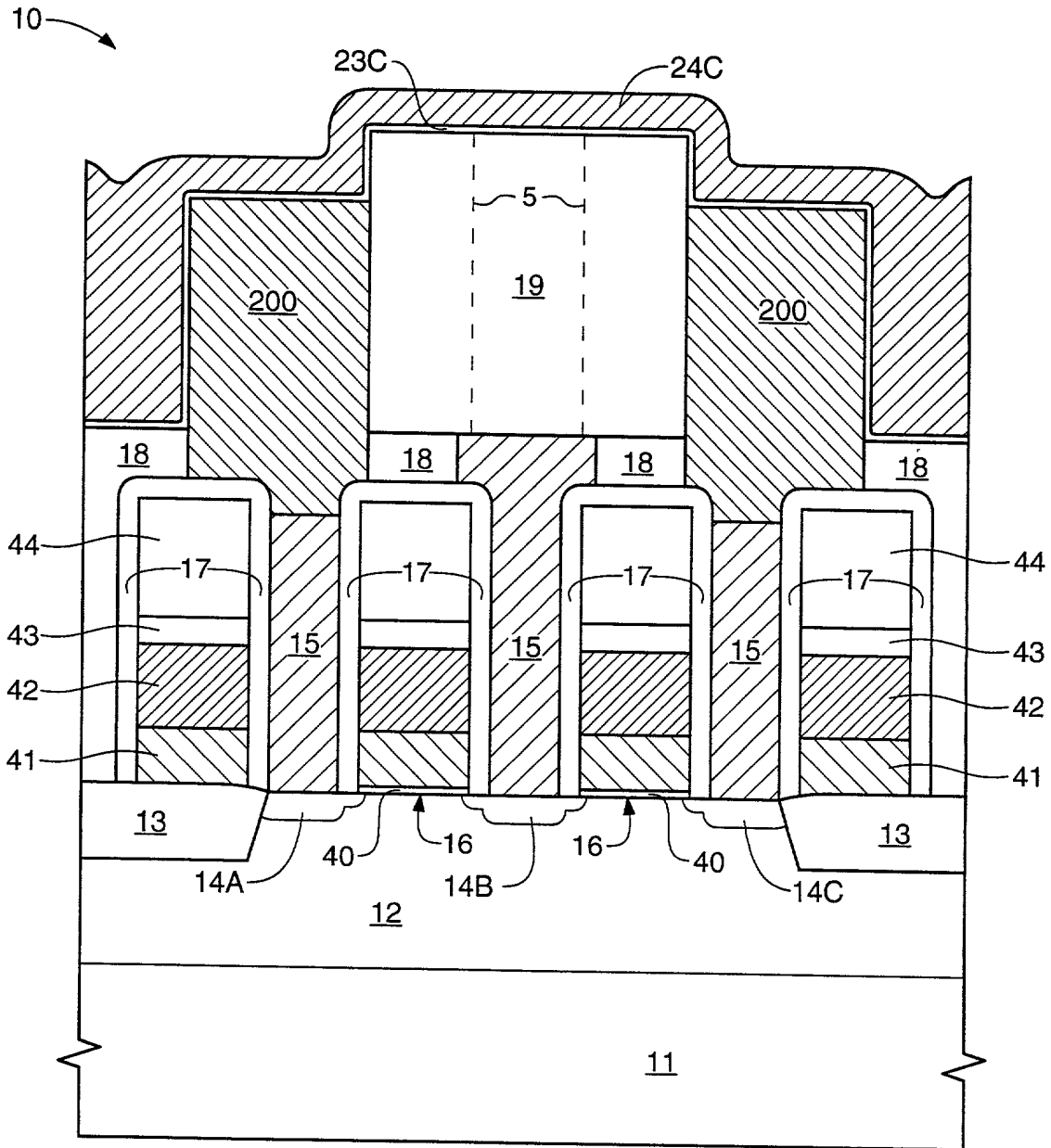


FIG. 16F

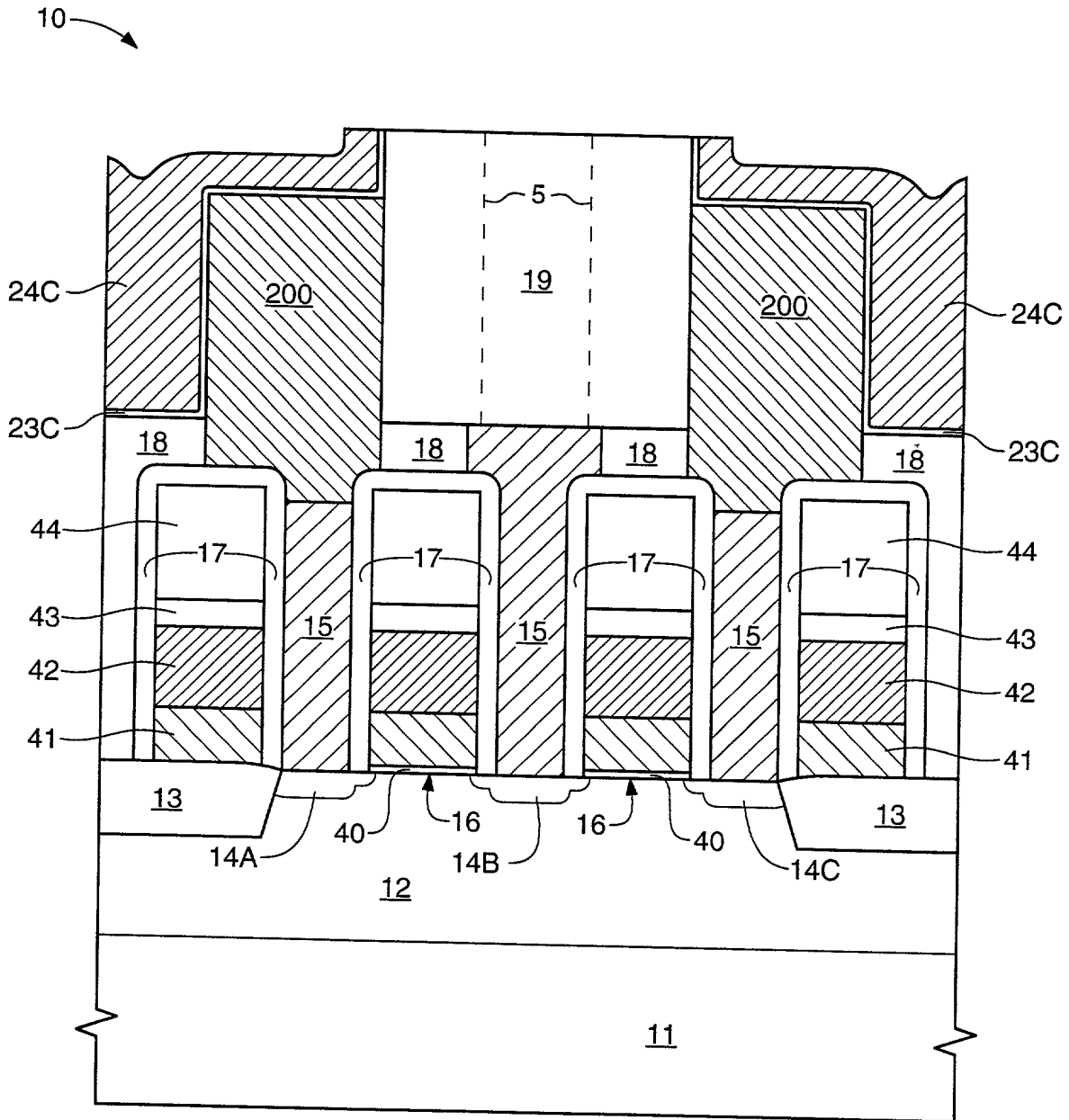


FIG. 16G

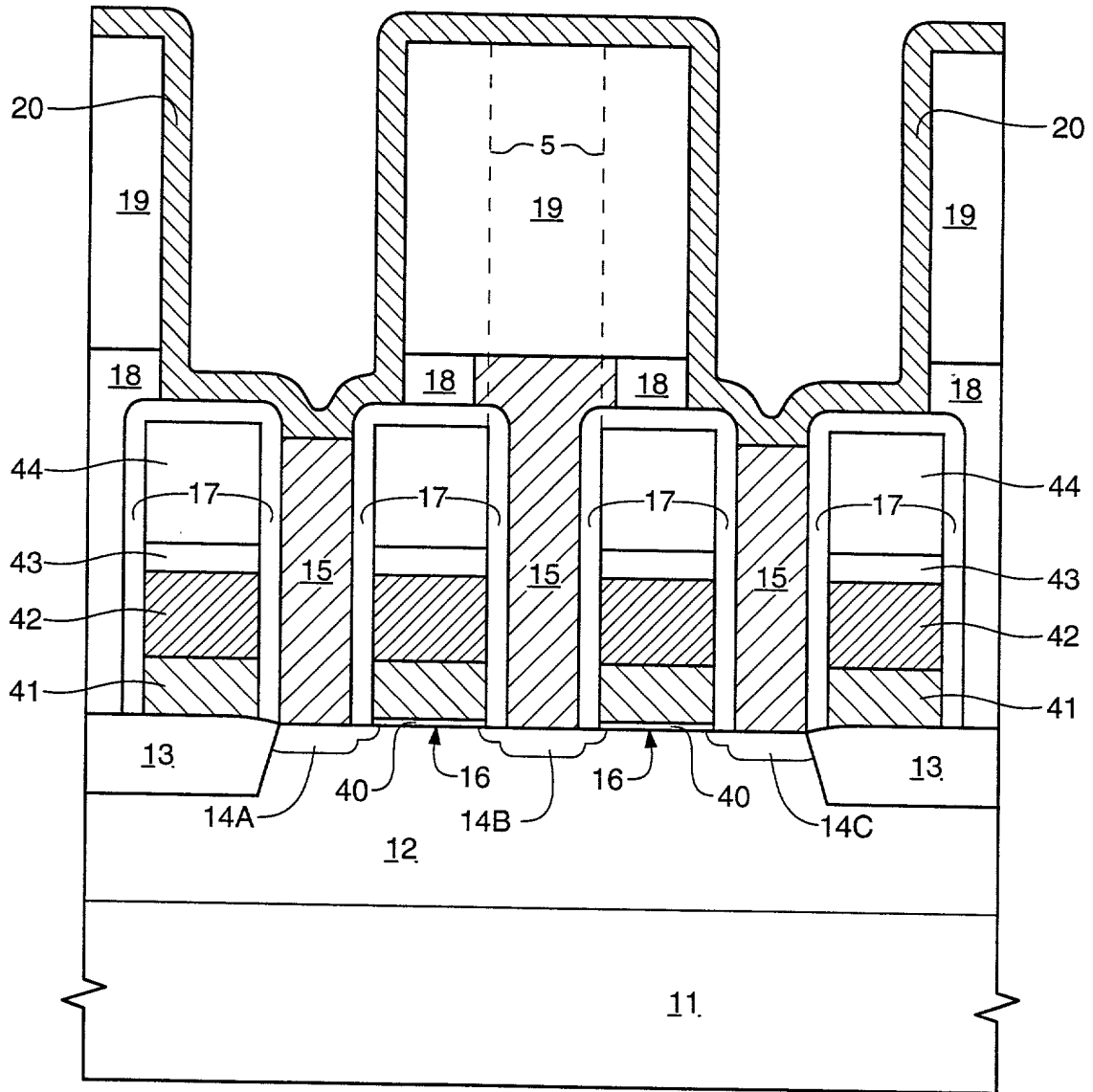


FIG. 17A

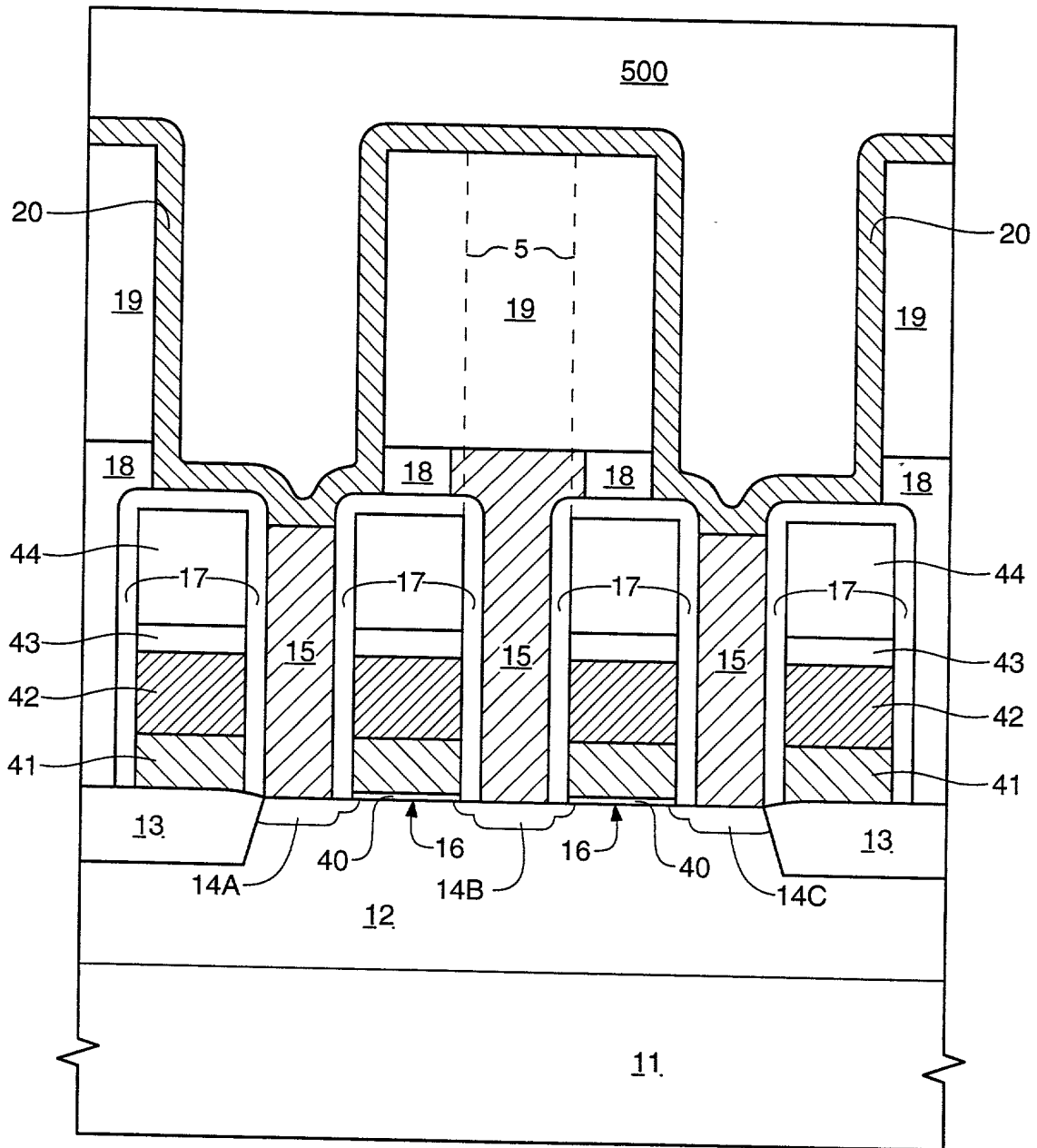


FIG. 17B

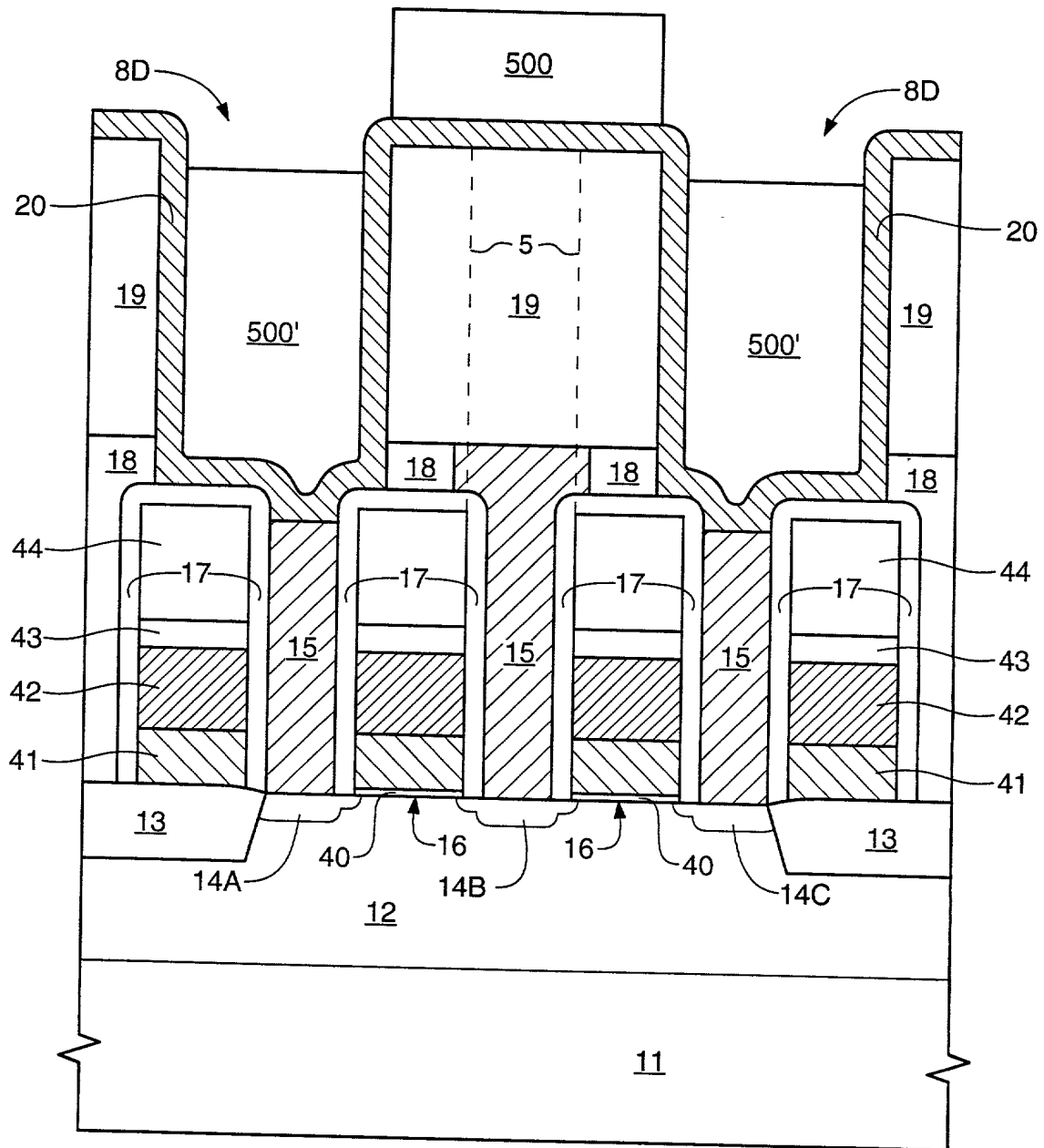
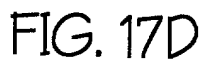


FIG. 17C



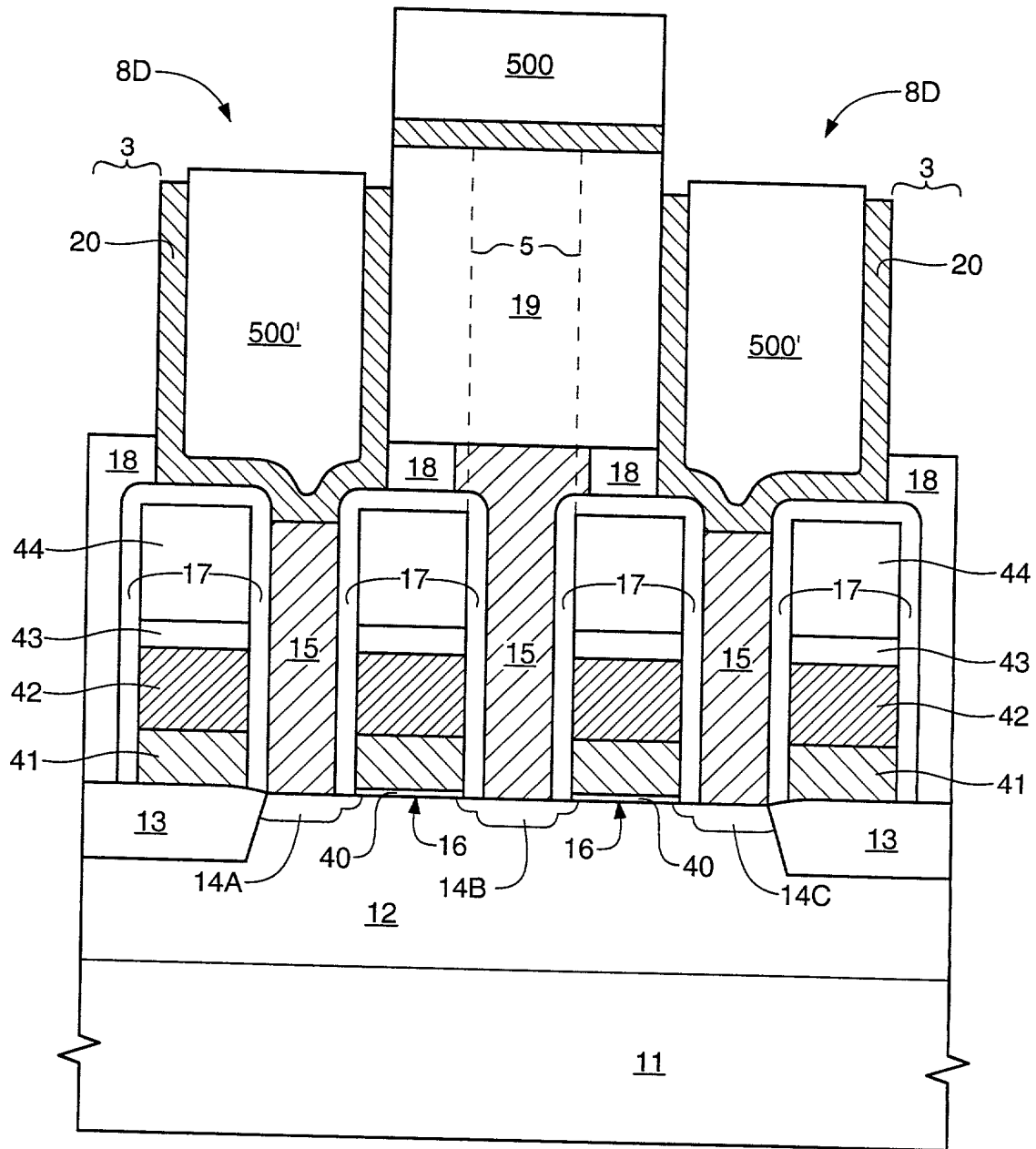


FIG. 17E



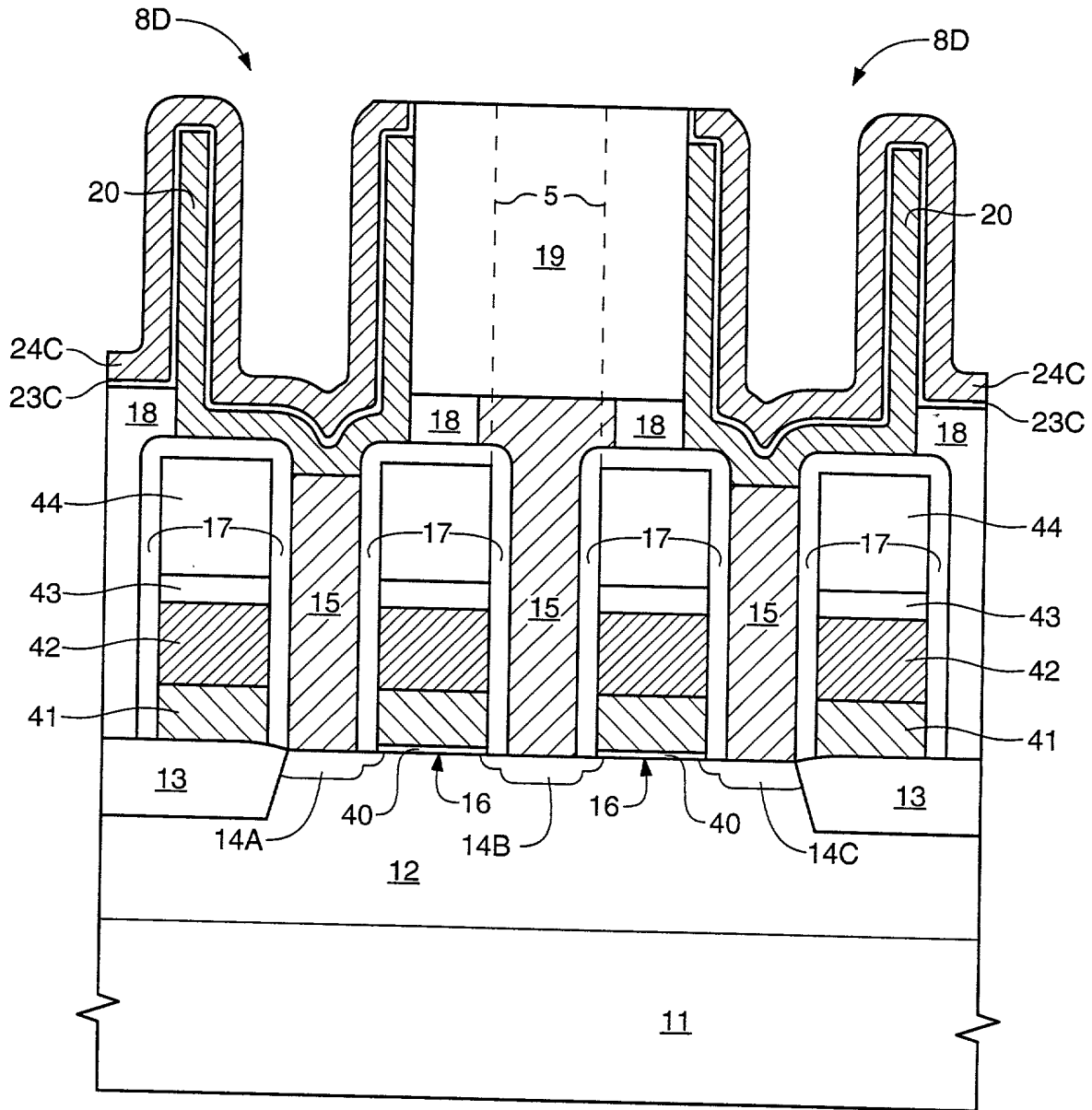
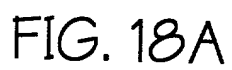
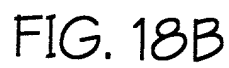


FIG. 17G





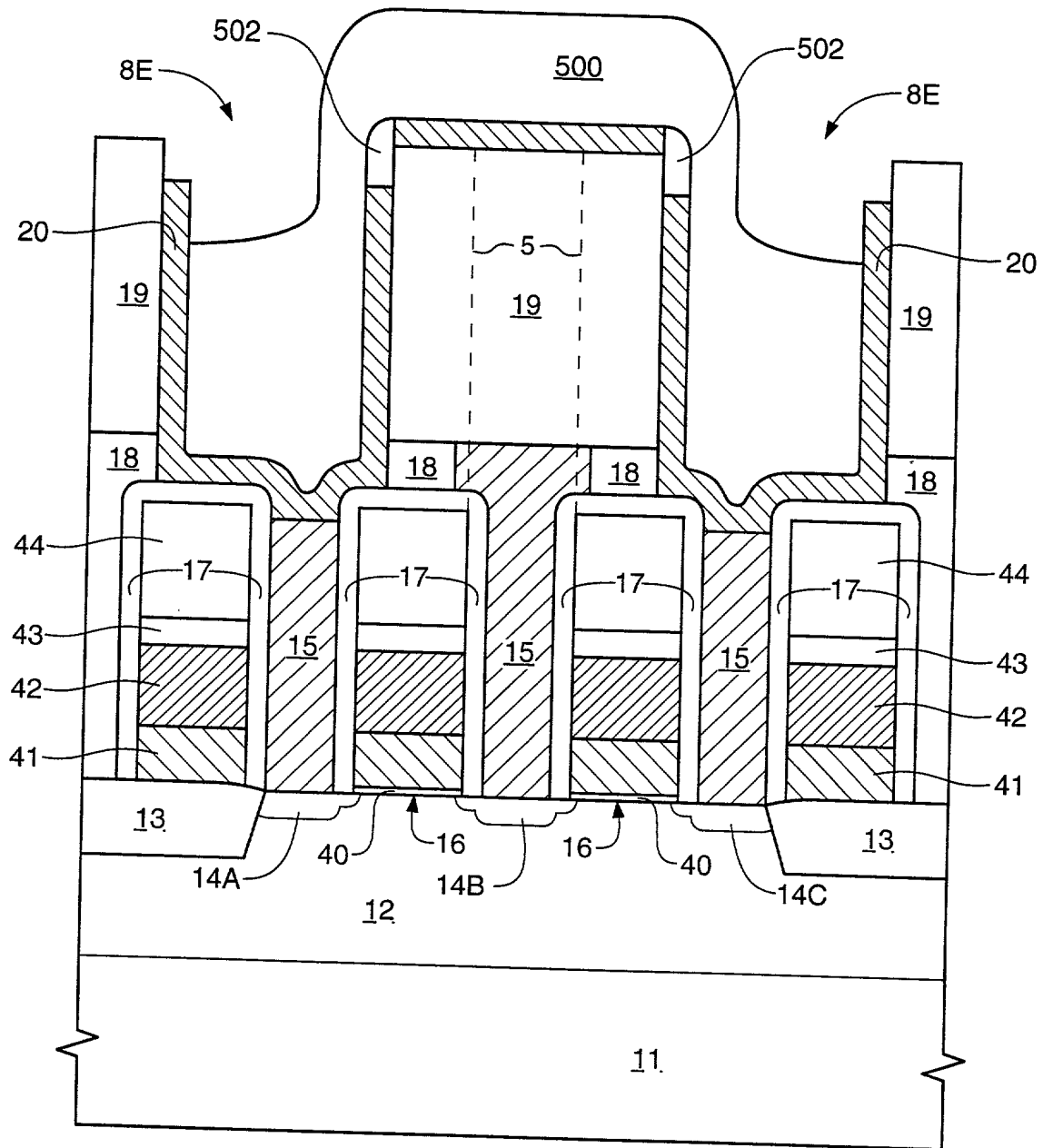


FIG. 18C

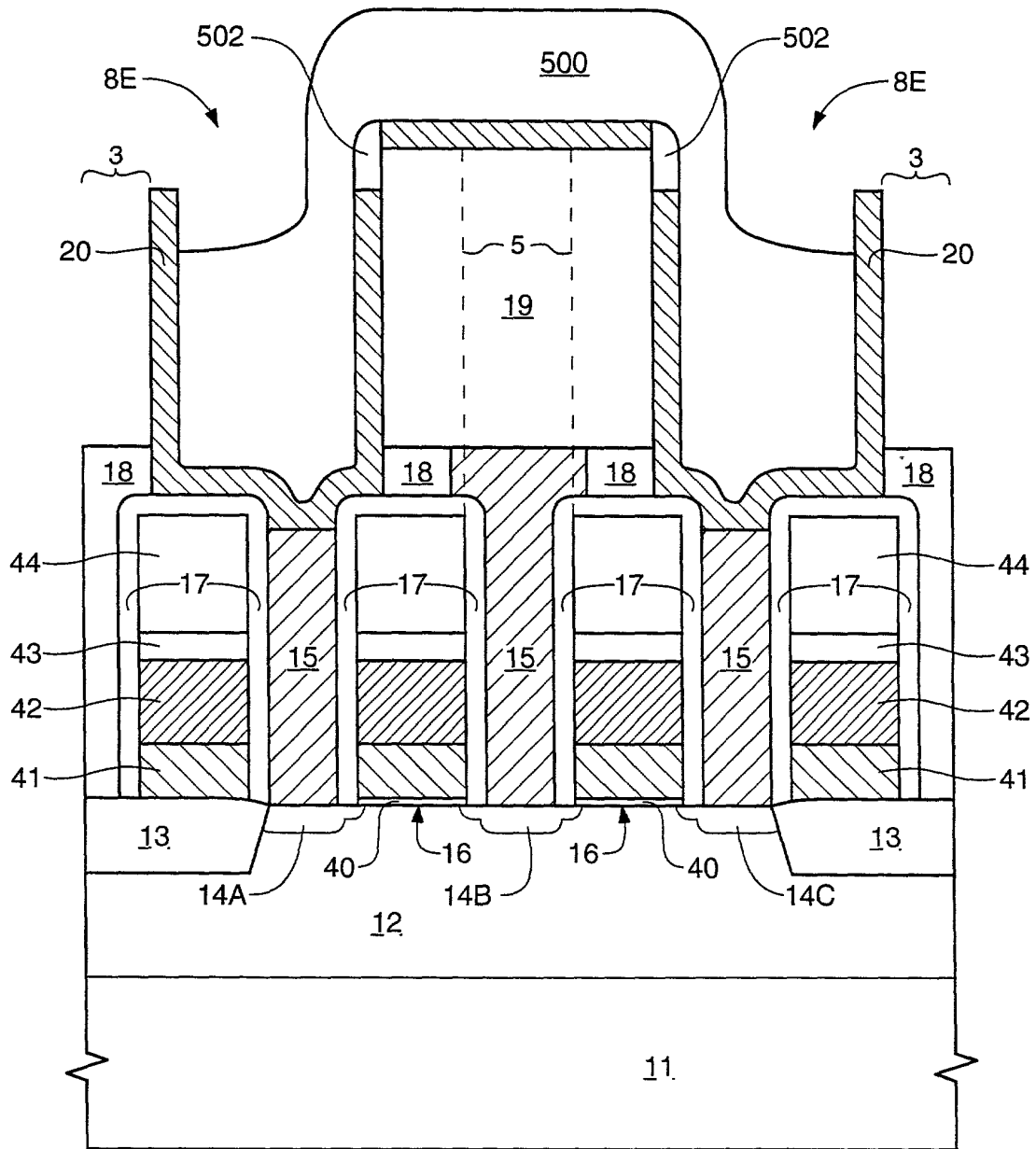
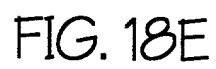
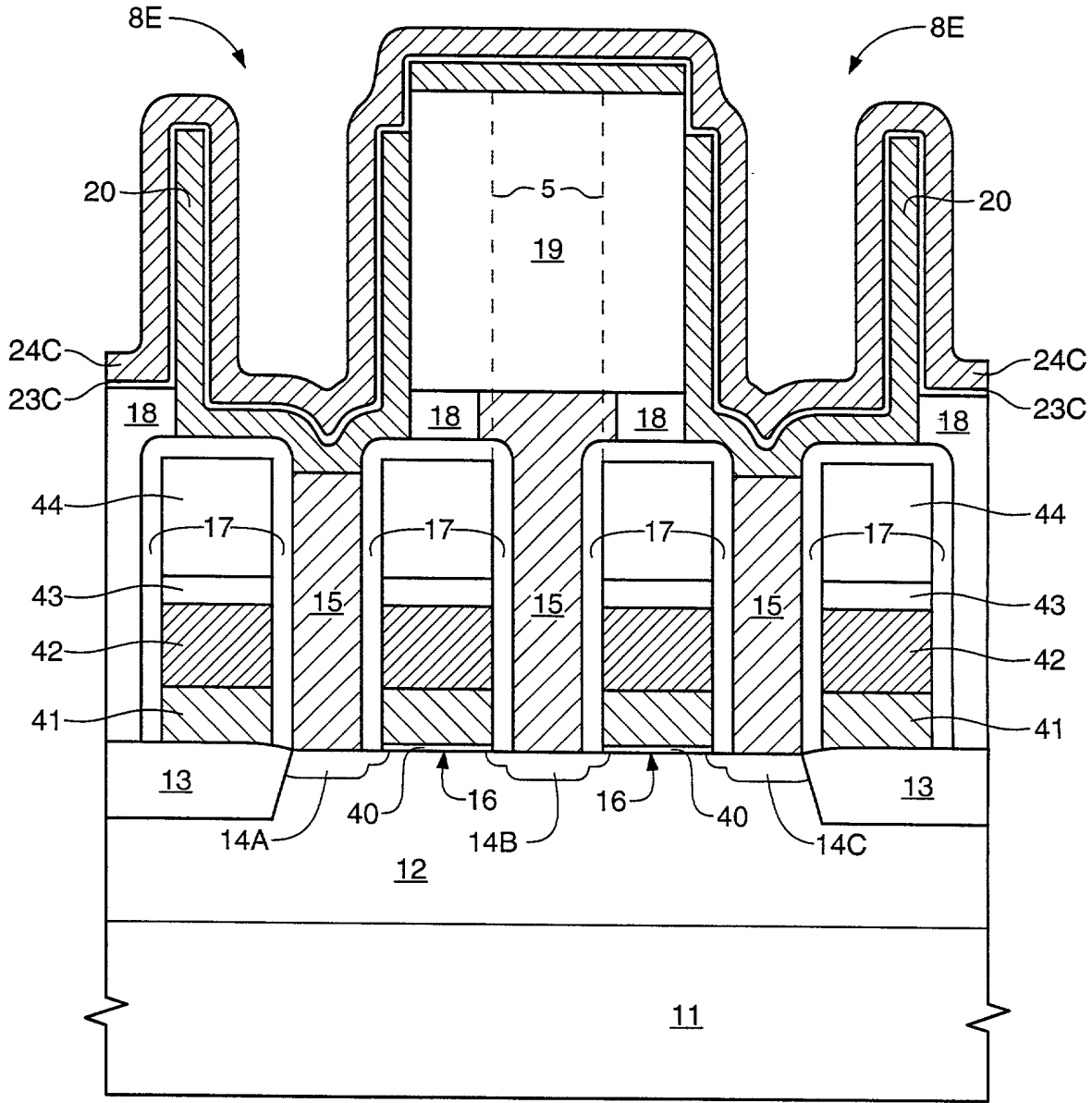


FIG. 18D





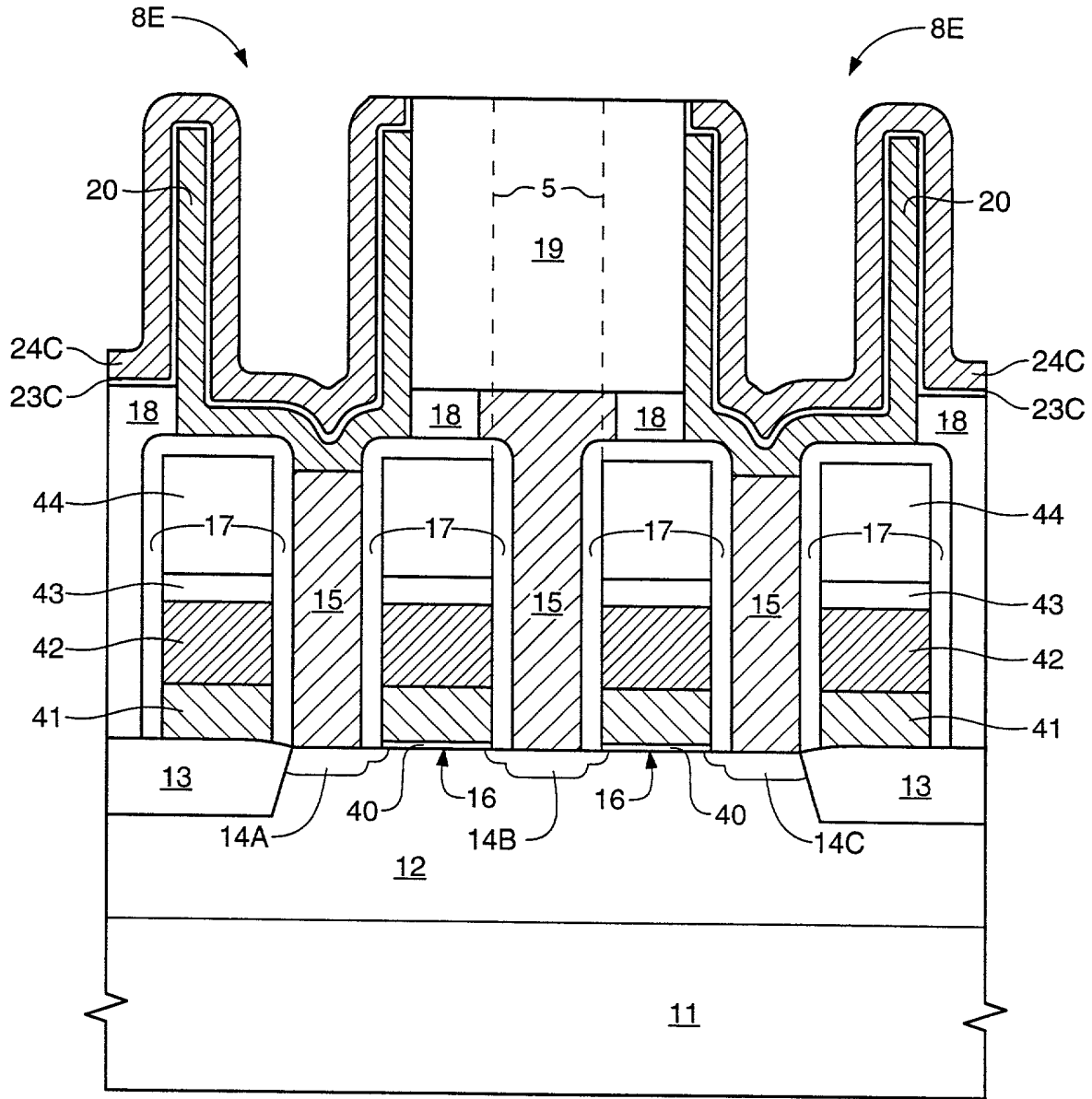


FIG. 18G

DECLARATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled CONTAINER CAPACITOR STRUCTURE AND METHOD OF FORMATION THEREOF, the specification of which:

X is attached hereto.

_____ was filed on _____, as Application Serial No. _____.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims.

I acknowledge the duty to disclose information which is material to patentability of the subject matter claimed in this application as "materiality" is defined in Title 37 of the Code of Federal Regulations, § 1.56.

I hereby claim the benefit of any earlier filing date in the United States to which I am entitled under Title 35 of the United States Code, § 120 and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35 of the United States Code, § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37 of the Code of Federal Regulations, § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

(Application Serial No.)

(Filing Date)


(Status)

Send correspondence to:

Charles Brantley, Reg. 38,086
Mail Stop 525
Micron Technology, Inc.
8000 S. Federal Way
Boise, Idaho 83716
(208) 368-4557

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Title 18 of the United States Code, § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of first or sole inventor: D. Mark Durcan

Inventor's Signature: 
(First, Middle Initial, Last)

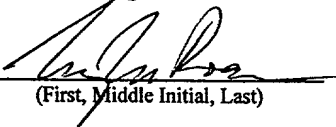
Date:

Residence Address: 4850 Boise River Lane
City, State, Country: Boise, Idaho 83706 United States of America

Citizenship: USA

Post Office Address: Same as residence address

Full name of additional inventor: Trung T. Doan

Inventor's Signature: 
(First, Middle Initial, Last)

Date:

Residence Address: 1574 Shenandoah Drive
City, State, Country: Boise, Idaho 83712-6668 United States of America

Citizenship: USA

Post Office Address: Same as residence address

Full name of additional inventor: Roger R. Lee

Inventor's Signature: 
(First, Middle Initial, Last)

Date:

Residence Address: 3936 N. Burnstead
City, State, Country: Boise, Idaho 83704 United States of America

Citizenship: USA

Post Office Address: Same as residence address

Full name of additional inventor: Fernando Gonzalez

Inventor's Signature: 
(First, Middle Initial, Last)

Date:

Residence Address: 2579 S. Flotilla Avenue
City, State, Country: Boise, Idaho 83706 United States of America

Citizenship: USA

Post Office Address: Same as residence address

001100-66629960

Full name of first or sole inventor: Er-Xuan Ping

Inventor's Signature:

Er-Xuan Ping
(First, Middle Initial, Last)

Date:

09/02/99

Residence Address:

2239 E. Chateau Drive

City, State, Country:

Meridian, Idaho 83642

United States of America

Citizenship:

USA

Post Office Address:

Same as residence address

001E80-6665560

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: D. Mark Durcan et al.

§ Atty. Docket: 98-1068.02

Serial No.:

Filed: August 31, 2000

For: CONTAINER CAPACITOR STRUCTURE
AND METHOD OF FORMATION THEREOF

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§ COMMISSIONER FOR PATENTS, WASHINGTON, D.C. 20231

Signature

ELECTION UNDER 37 C.F.R. §§ 3.71 AND 3.73 AND POWER OF ATTORNEY

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

The undersigned, being Assignee of the entire interest in the above-identified application by virtue of an Assignment recorded in the United States Patent and Trademark Office as set forth below or filed herewith, hereby elects, under 37 C.F.R. § 3.71, to prosecute the application to the exclusion of the inventor(s).

The Assignee hereby revokes any previous Powers of Attorney and appoints: Charles B. Brantley, II, Reg. No. 38,086; Michael L. Lynch, Reg. No. 30,871; Walter D. Fields, Reg. No. 37,130; Kevin D. Martin, Reg. No. 37,882; and David J. Paul, Reg. No. 34,692 as its attorney or agent, with full power of substitution and revocation, to prosecute the application, to make alterations and amendments therein, to transact all business in the Patent and Trademark Office in connection therewith, to receive any Letters Patent, and for one year after issuance of such Letters Patent to file any request for a certificate of correction that may be deemed appropriate.

Pursuant to 37 C.F.R. § 3.73, the undersigned duly authorized designee of Assignee certifies that the evidentiary documents have been reviewed, specifically the Assignment to MICRON TECHNOLOGY, INC., referenced below, and certifies that to the best of my knowledge and belief, title remains in the name of the Assignee.

Assignment:

 Filed concurrently herewith for
recording, a copy of which is
attached hereto.


 X Previously recorded on: 9/2/99, at
Reel: 010225, Frame: 0728

Please direct all communications as follows:

Charles B. Brantley, Mail Stop 525
MICRON TECHNOLOGY, INC.
8000 S. Federal Way
Boise, ID 83716-9632
(208) 368-4557

ASSIGNEE: MICRON TECHNOLOGY, INC.

Date: 8-30-00

By: 
Michael L. Lynch, Reg. 30,871
Chief Patent Counsel